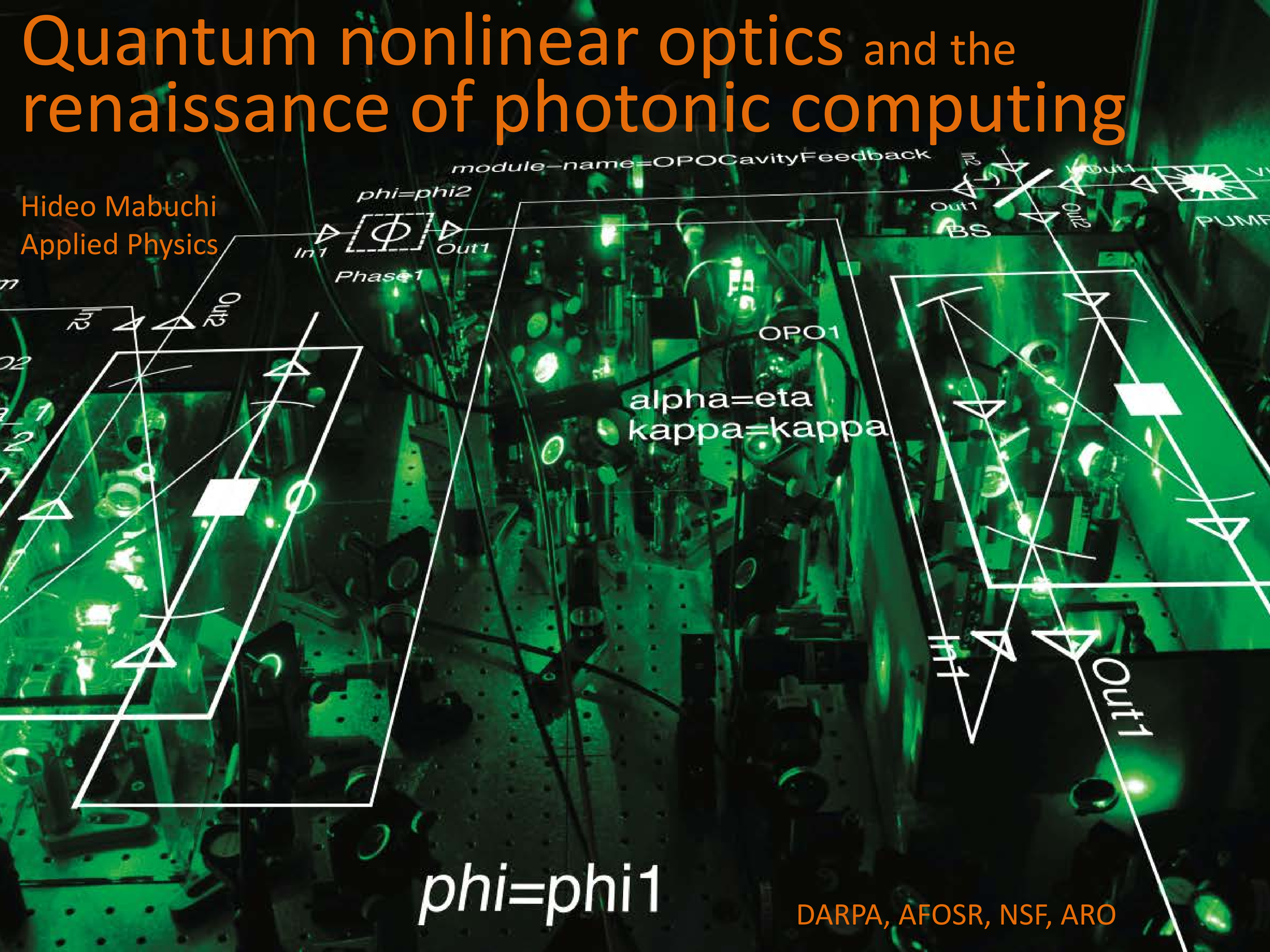
Quantum nonlinear optics and the renaissance of photonic computing

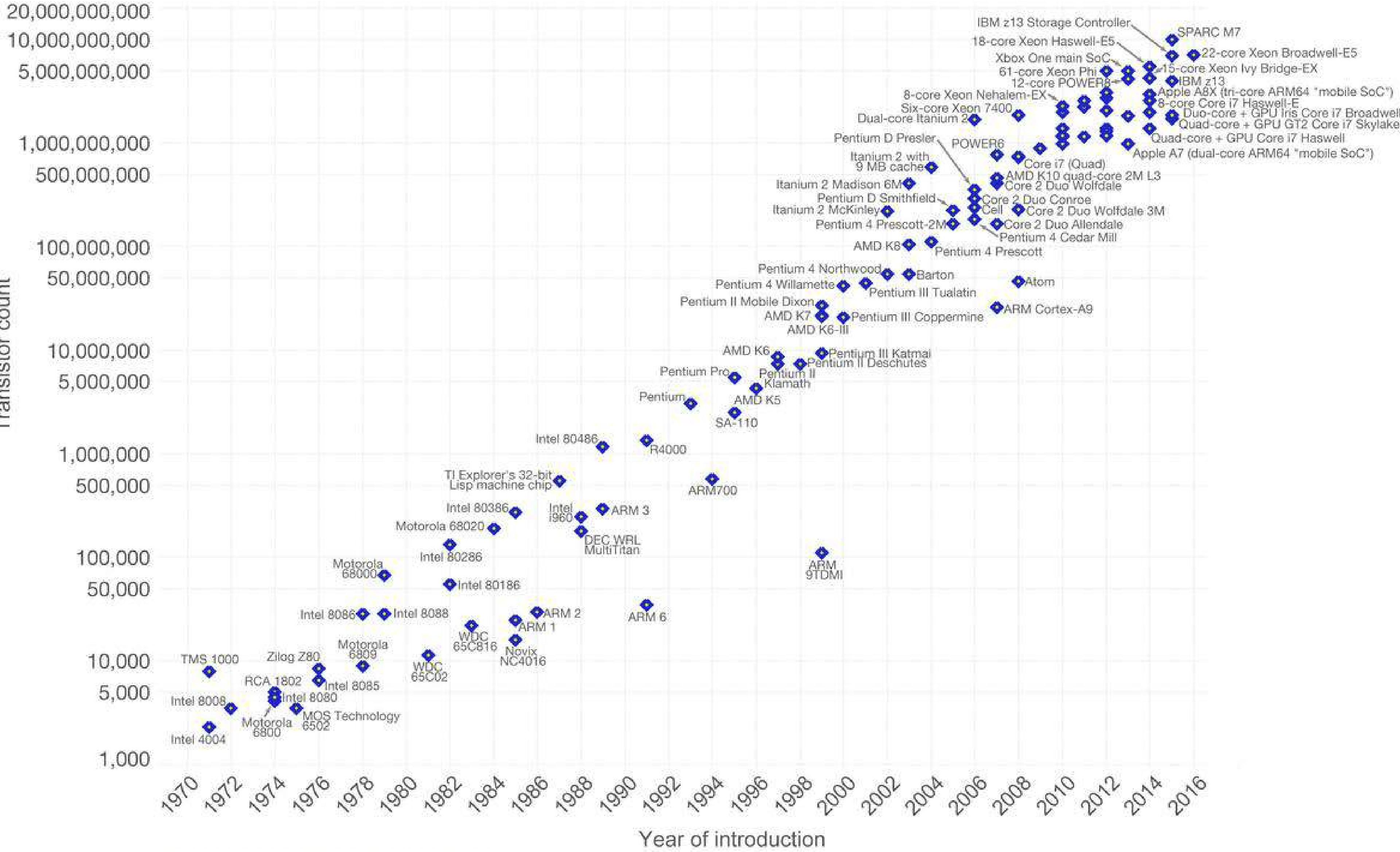
Hideo Mabuchi
Applied Physics



DARPA, AFOSR, NSF, ARO

Moore's Law – The number of transistors on integrated circuit chips (1971-2016)

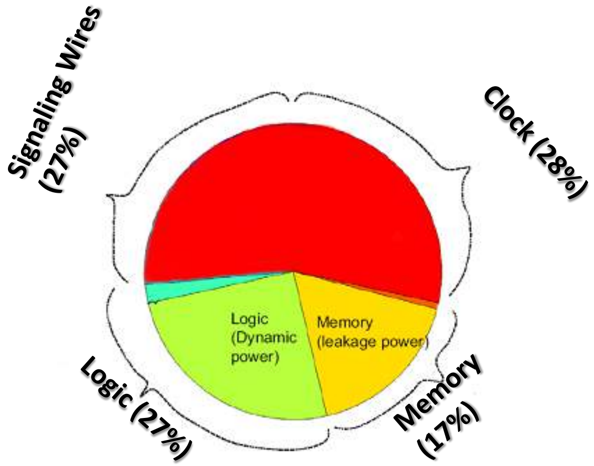
Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are trongly linked to Moore's law.



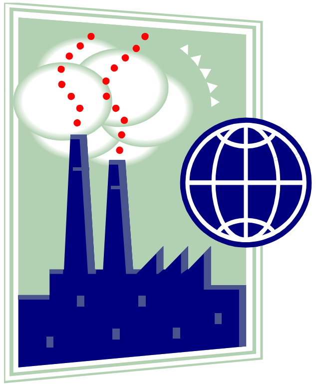
ata source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
he data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Energy efficiency in high performance computing

D. A. B. Miller, Proc. IEEE **97**, 1166 (2009)



- Interconnect power limits chip performance
  - ~ 50% of µprocessor power was interconnects in 2002
    - Expected to rise to 80%
    - Chip power limited to ~ 200 W from now on
- System power is financially significant
  - The cost of powering a server is now comparable to the purchase cost of the server hardware
- System power is environmentally significant
  - Data centers consumed ~ 1.5% of US electricity in 2006
    - Power expected to double by 2011
    - Server interconnect power already larger than solar power generation in the US
    - Information technology has as much energy and carbon impact as the airline industry
- Conclusion - Any new interconnect solution must take less power, but optics fundamentally can do this



Guardian Environment Network
Environment

'Tsunami of data' could consume one fifth of global electricity by 2025

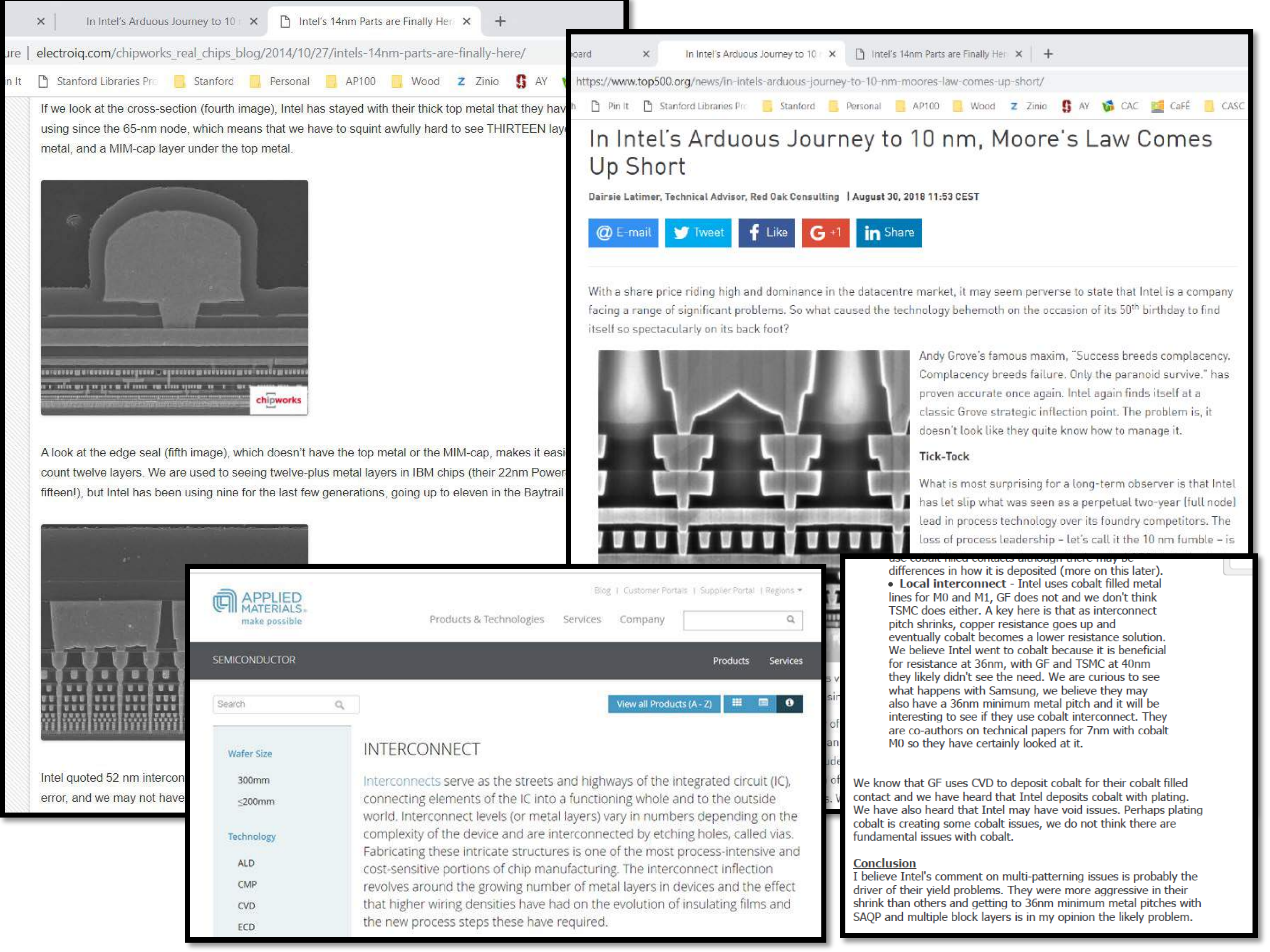
Billions of internet-connected devices could produce 3.5% of global emissions within 10 years and 14% by 2040, according to new research, reports Climate Home News

Climate Home News, part of the Guardian Environment Network
Mon 11 Dec 2017 08.27 EST

This article is over **10 months old**

A Google data centre. US researchers expect power consumption to triple in the next five years as one billion more people come online in developing countries. Photograph: Google/Rex

The communications industry could use 20% of all the world's electricity by 2025, hampering attempts to meet climate change targets and straining grids as demand by power-hungry server farms storing digital data from billions of smartphones, tablets and internet-connected devices grows exponentially.



If we look at the cross-section (fourth image), Intel has stayed with their thick top metal that they hav using since the 65-nm node, which means that we have to squint awfully hard to see THIRTEEN lay metal, and a MIM-cap layer under the top metal.

A look at the edge seal (fifth image), which doesn't have the top metal or the MIM-cap, makes it easi count twelve layers. We are used to seeing twelve-plus metal layers in IBM chips (their 22nm Power fifteen!), but Intel has been using nine for the last few generations, going up to eleven in the Baytrail

Intel quoted 52 nm intercon error, and we may not have

In Intel's Arduous Journey to 10 nm, Moore's Law Comes Up Short

Dairsie Latimer, Technical Advisor, Red Oak Consulting | August 30, 2018 11:53 CEST

With a share price riding high and dominance in the datacentre market, it may seem perverse to state that Intel is a company facing a range of significant problems. So what caused the technology behemoth on the occasion of its 50th birthday to find itself so spectacularly on its back foot?

Andy Grove's famous maxim, "Success breeds complacency. Complacency breeds failure. Only the paranoid survive." has proven accurate once again. Intel again finds itself at a classic Grove strategic inflection point. The problem is, it doesn't look like they quite know how to manage it.

Tick-Tock

What is most surprising for a long-term observer is that Intel has let slip what was seen as a perpetual two-year (full node) lead in process technology over its foundry competitors. The loss of process leadership – let's call it the 10 nm fumble – is

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INTERCONNECT

Interconnects serve as the streets and highways of the integrated circuit (IC), connecting elements of the IC into a functioning whole and to the outside world. Interconnect levels (or metal layers) vary in numbers depending on the complexity of the device and are interconnected by etching holes, called vias. Fabricating these intricate structures is one of the most process-intensive and cost-sensitive portions of chip manufacturing. The interconnect inflection revolves around the growing number of metal layers in devices and the effect that higher wiring densities have had on the evolution of insulating films and the new process steps these have required.

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differences in how it is deposited (more on this later).

- **Local interconnect** - Intel uses cobalt filled metal lines for M0 and M1, GF does not and we don't think TSMC does either. A key here is that as interconnect pitch shrinks, copper resistance goes up and eventually cobalt becomes a lower resistance solution. We believe Intel went to cobalt because it is beneficial for resistance at 36nm, with GF and TSMC at 40nm they likely didn't see the need. We are curious to see what happens with Samsung, we believe they may also have a 36nm minimum metal pitch and it will be interesting to see if they use cobalt interconnect. They are co-authors on technical papers for 7nm with cobalt M0 so they have certainly looked at it.

We know that GF uses CVD to deposit cobalt for their cobalt filled contact and we have heard that Intel deposits cobalt with plating. We have also heard that Intel may have void issues. Perhaps plating cobalt is creating some cobalt issues, we do not think there are fundamental issues with cobalt.

Conclusion

I believe Intel's comment on multi-patterning issues is probably the driver of their yield problems. They were more aggressive in their shrink than others and getting to 36nm minimum metal pitches with SAQP and multiple block layers is in my opinion the likely problem.

(nano)Photonic integration: on the roadmap?

Large Scale Integrated Photonics for Twenty-Fi
Century Information Technologies

A “Moore’s Law” for Optics

Authors Authors and affiliations

Raymond G. Beausoleil

Electronic-Photonic Design Automatio

The Electronic-Photonic Design Automation (EPDA) TWG focuses on improving design methodologies for scalable integrated electronic/photonic design. One of the overarching goals for improved methodologies and design tools (e.g., EDA and PDA software) is to enable the many electronics IC design teams of the world to integrate photonic functions into their systems/ASICs/SoCs without requiring low-level physics design and photonics PhDs on their staff (i.e., to make integrated photonics design easier by putting the low-level physics burden into the design tools and models). Another goal is enabling a robust photonics IP market. This includes analyzing existing methodologies and defining better ways (or standards) for the various forms of design data to move between the various design “steps” of a methodology.

Attojoule Optoelectronics for Low Energy Devices

David A. B. Miller

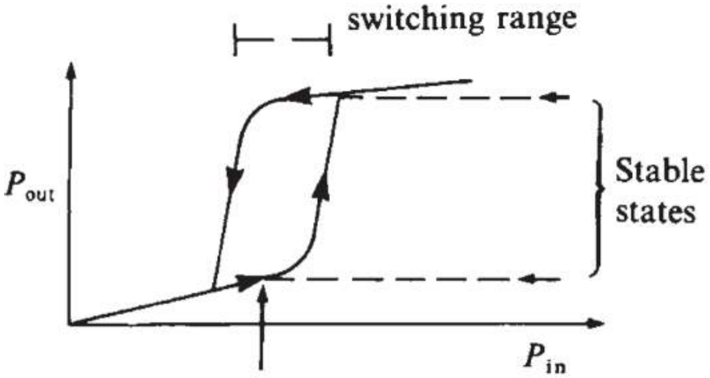
Joint European Platform for Photonic Integration of Components and Circuits

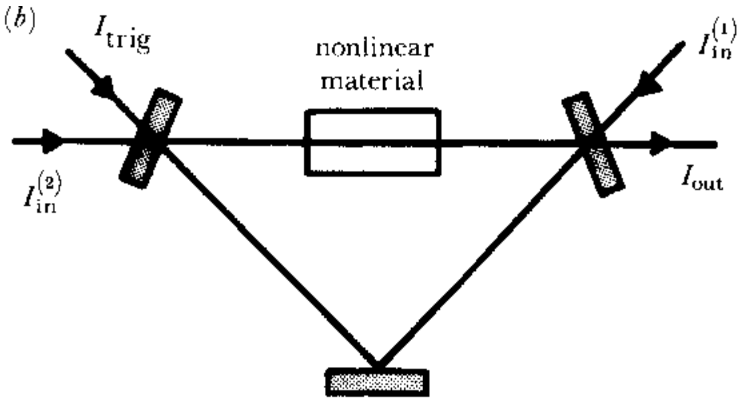
The road to a multi-billion Euro market

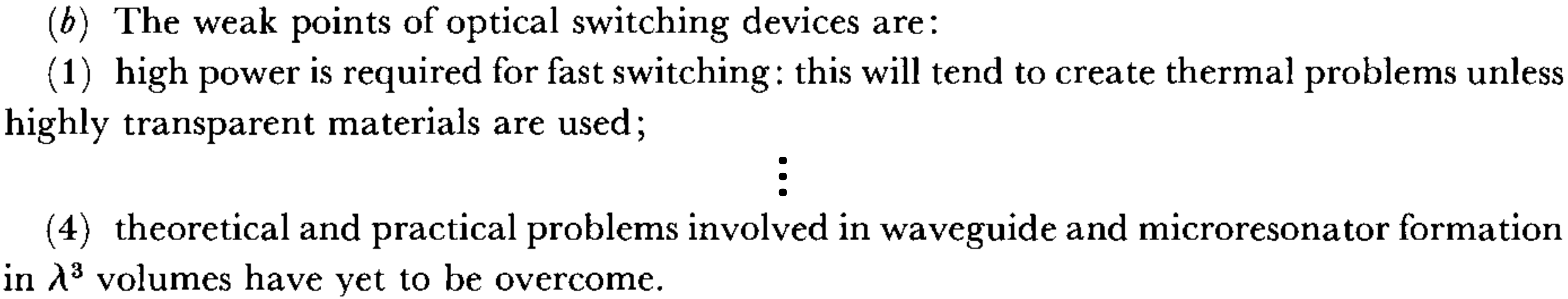
in Integrated Photonics

Nonlinear nanophotonics: back to the future?

P. W. Smith, Phil. Trans. R. Soc. Lond. A **313**, 349 (1984)





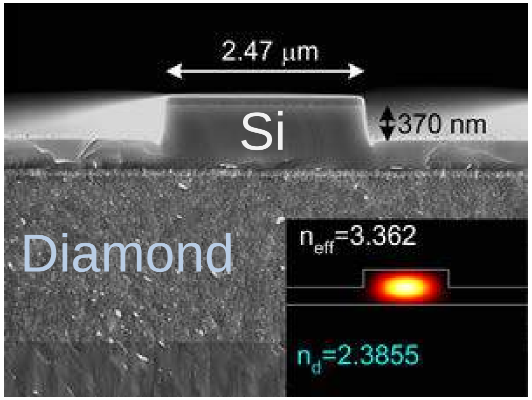


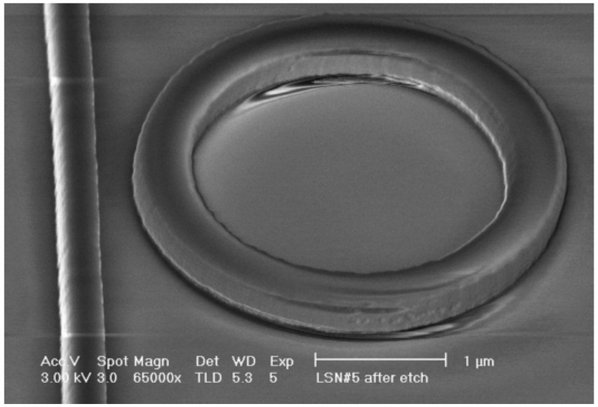
(*b*) The weak points of optical switching devices are:

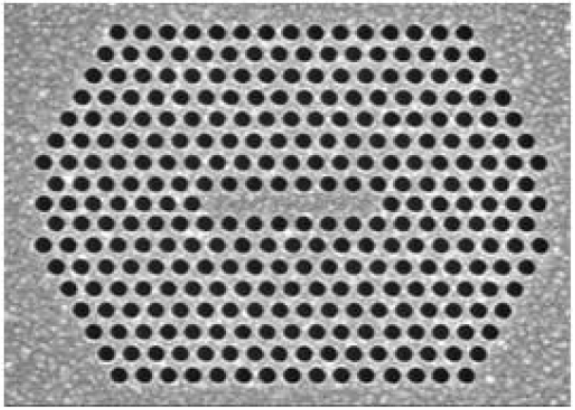
(1) high power is required for fast switching: this will tend to create thermal problems unless highly transparent materials are used;

⋮

(4) theoretical and practical problems involved in waveguide and microresonator formation in λ^3 volumes have yet to be overcome.

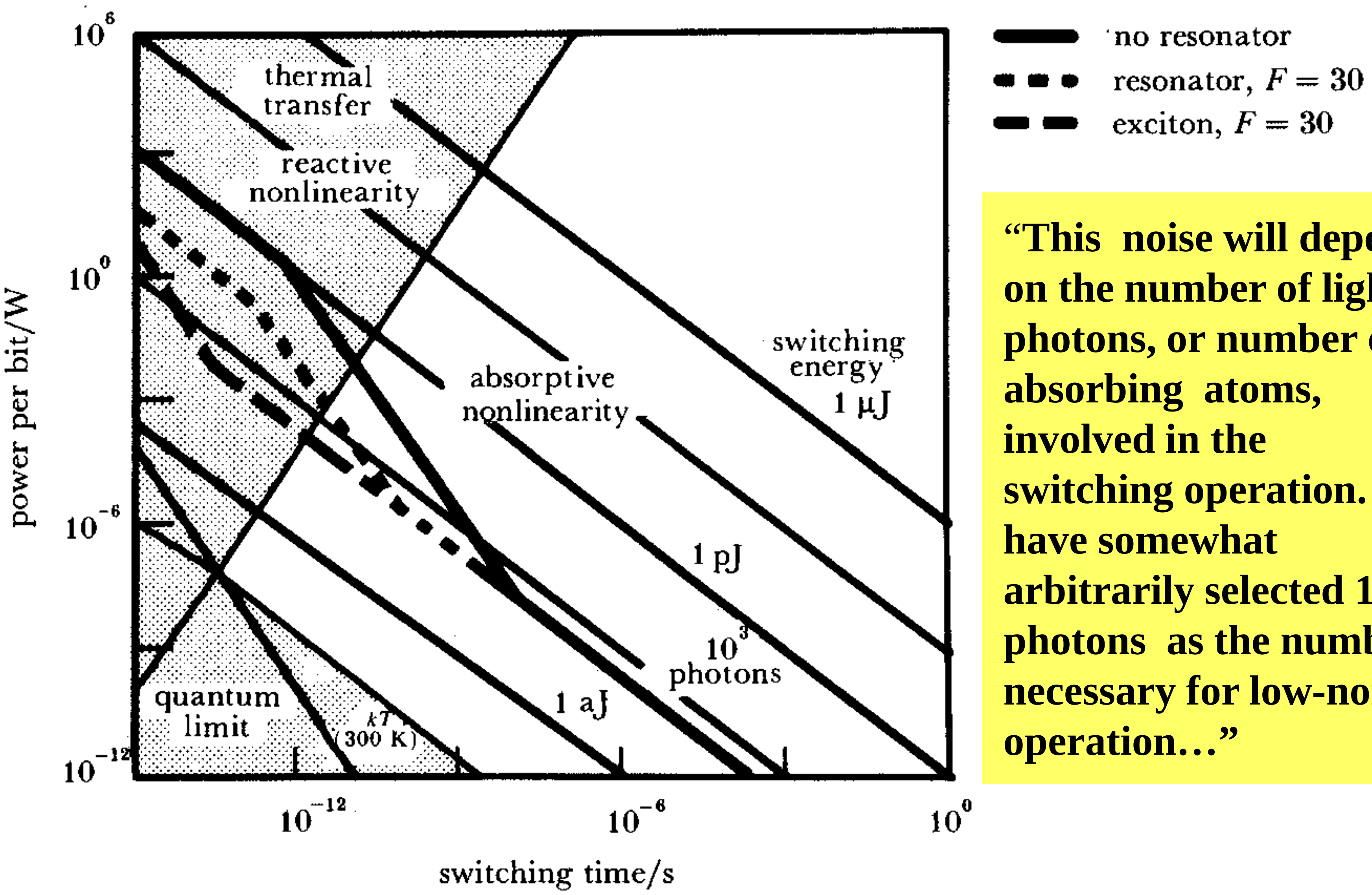






Quantum noise of classical switching devices

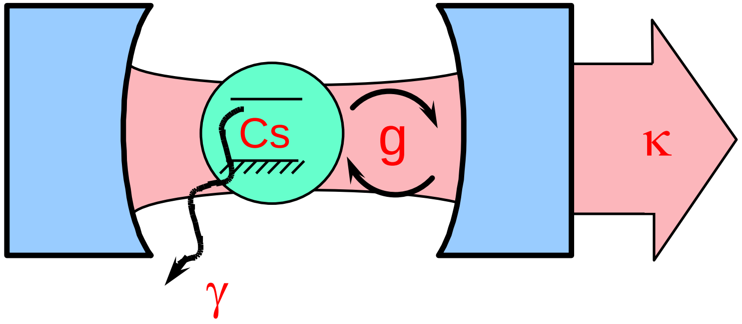
P. W. Smith, Phil. Trans. R. Soc. Lond. A **313**, 349 (1984)



"This noise will depend on the number of light photons, or number of absorbing atoms, involved in the switching operation. I have somewhat arbitrarily selected 10^3 photons as the number necessary for low-noise operation…"

Cavity QED with strong coupling

H. J. Kimble, Physica Scripta **176**, 127 (1998)



Critical photon number

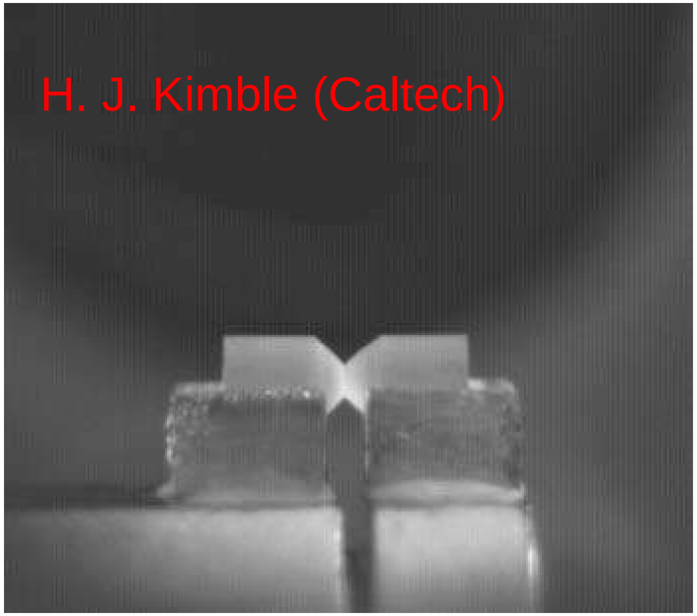
$$m_0 \approx \frac{\gamma^2}{2g^2} < 1$$

Nonlinear optics with
one photon per mode

Critical atom number

$$N_0 \approx \frac{2\gamma\kappa}{g^2} < 1$$

Single-atom switching of
optical cavity response


H. J. Kimble (Caltech)

Experiment: $m_0 \approx 3\times10^{-4}$ $N_0 \approx 6\times10^{-3}$

Projected: $m_0 \approx 6\times10^{-6}$ $N_0 \approx 2\times10^{-4}$

A. Scherer (Caltech)

Projected: $m_0 \approx 8\times10^{-9}$ $N_0 \approx 6\times10^{-5}$

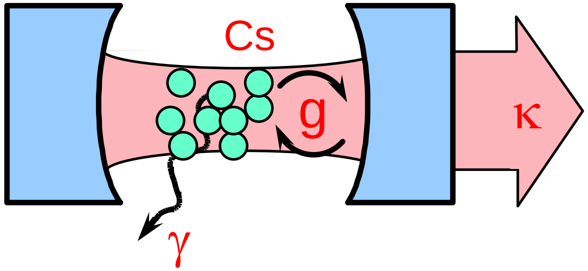
Quantum fluctuations in absorptive bistability

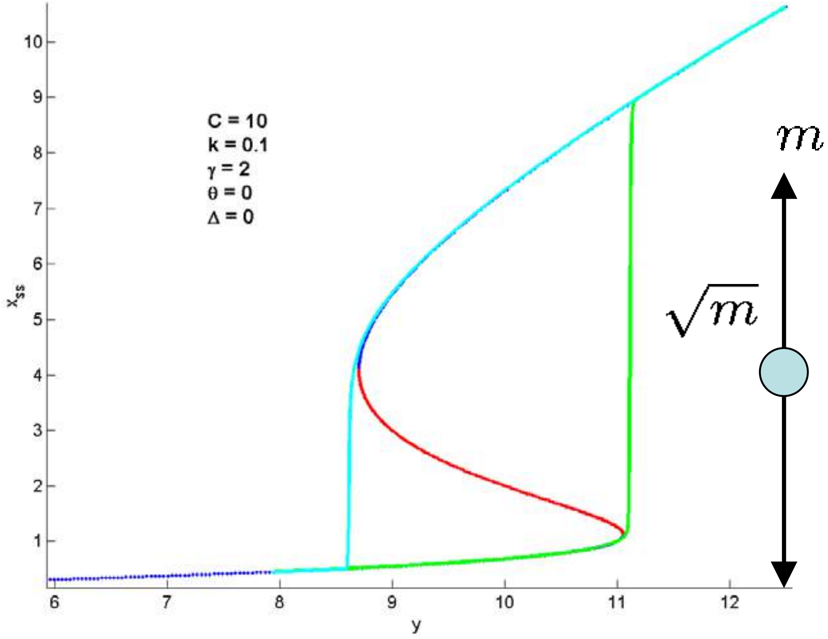
C. Savage and H. J. Carmichael IEEE J. Quantum Electron. **24**, 1495 (1988)

$$C = \frac{Ng^2}{2\kappa\gamma_\perp}$$

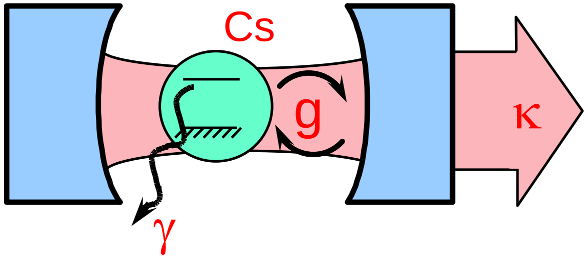
weak coupling

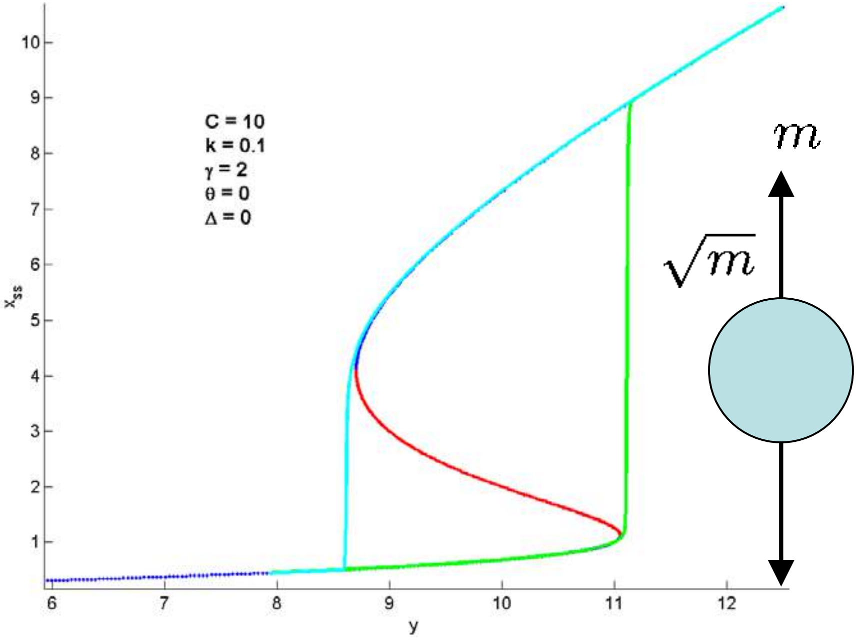
strong coupling





semi-classical nonlinear dynamics

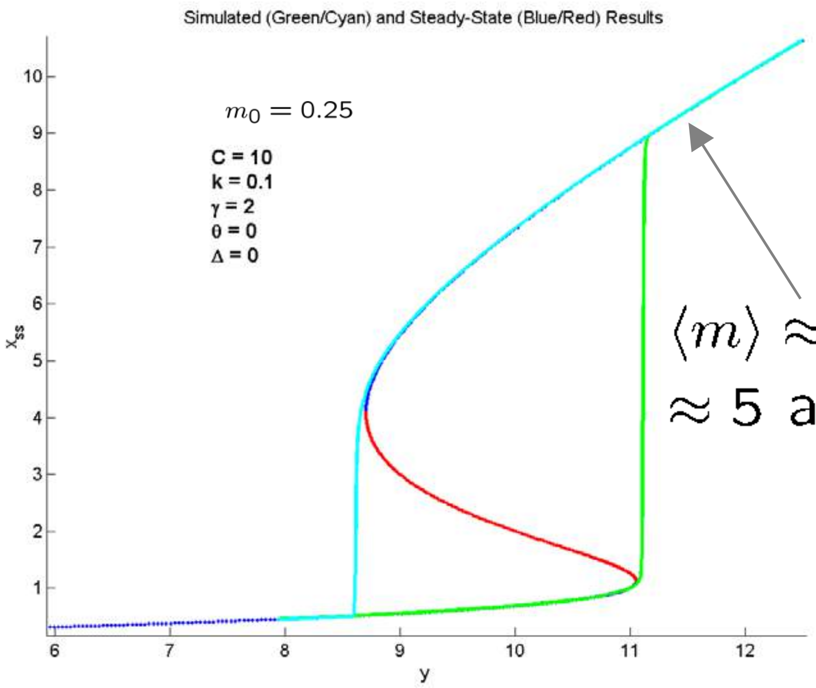




un-localized in phase portrait

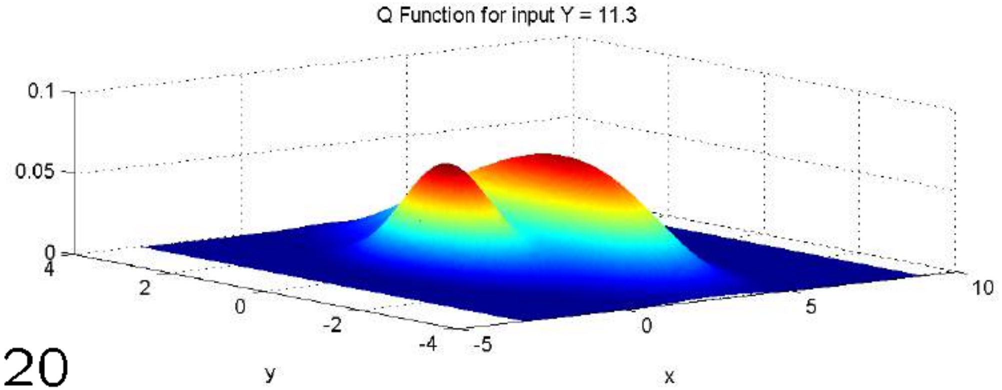
Single-atom absorptive “bistability”

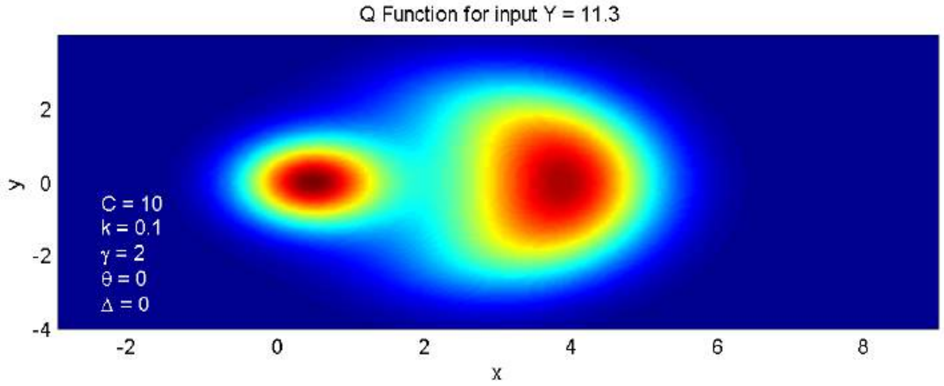
M. Armen and HM, PRA **73**, 063801 (2006)

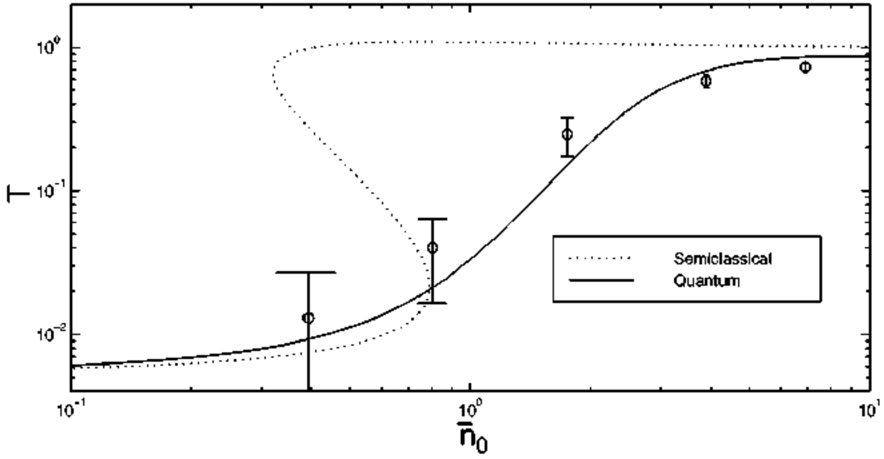


$\langle m \rangle \approx 20$

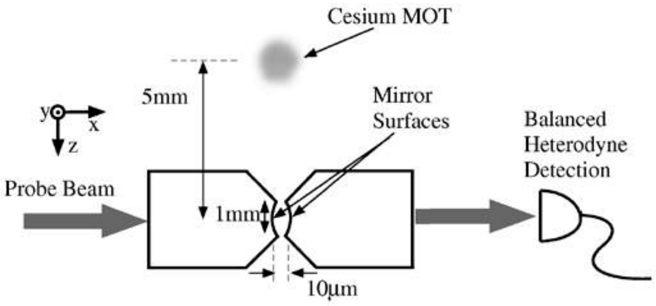
≈ 5 aJ





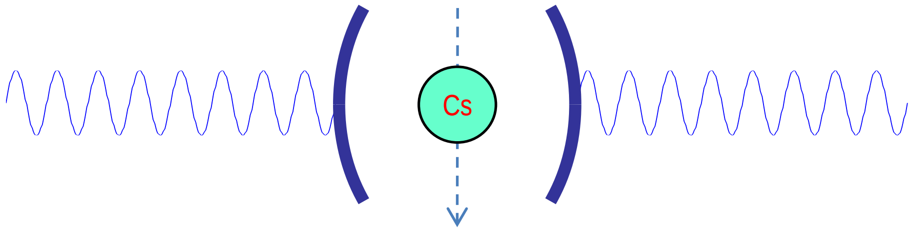


← Kimble and co-workers (‘98)

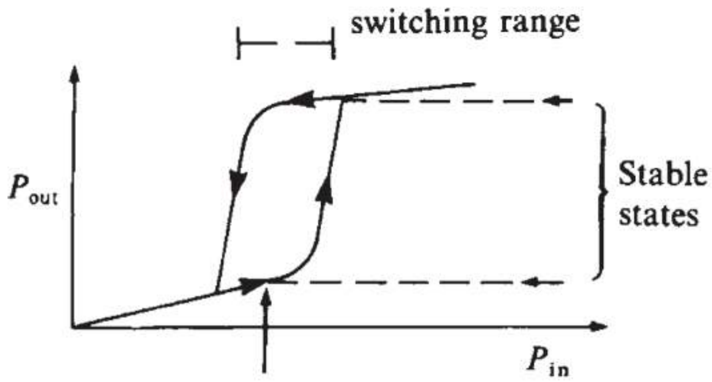


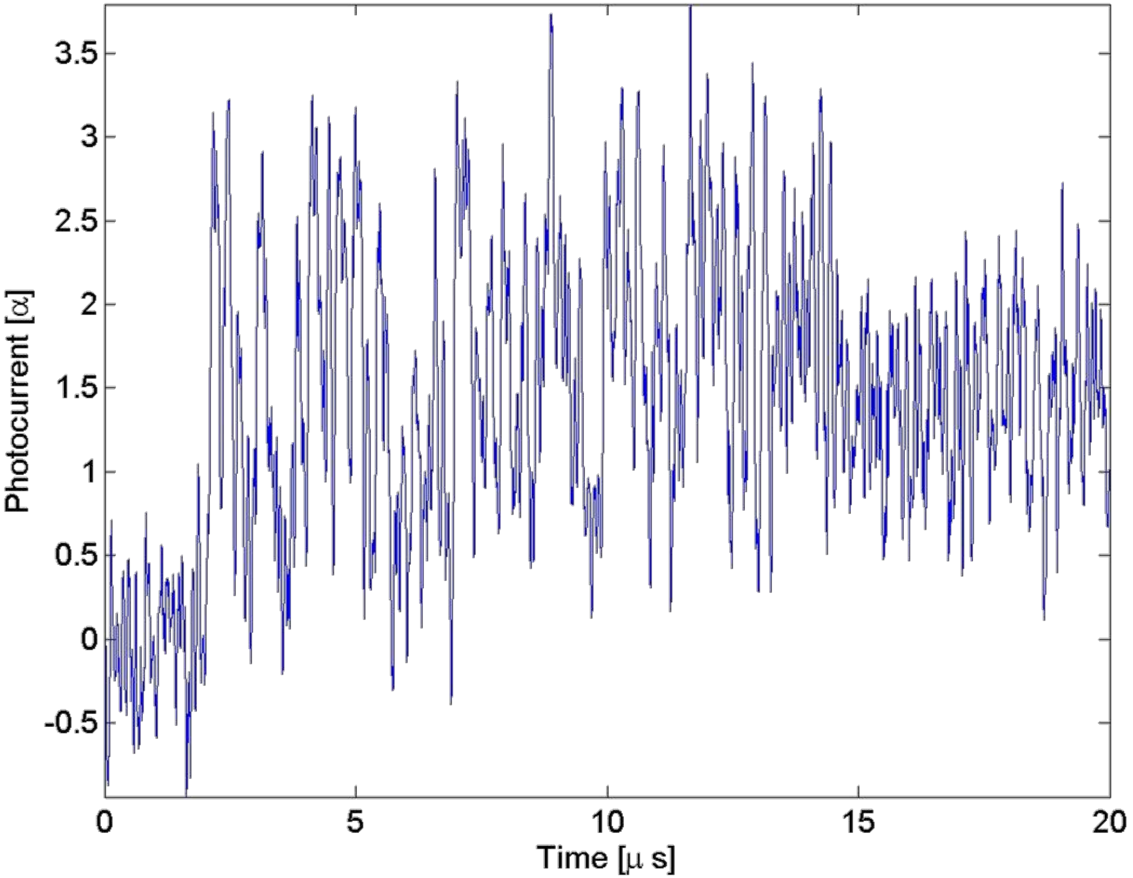
Spontaneous switching in attojoule “bistability”

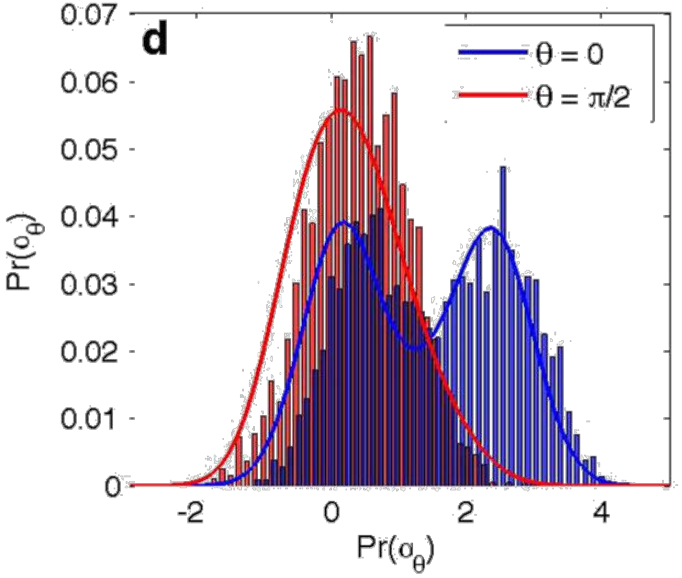
J. Kerckhoff, M. A. Armen and HM, Opt. Express **19**, 24468 (2011)



P. W. Smith, Phil. Trans. R. Soc. Lond. A **313**, 349 (1984)

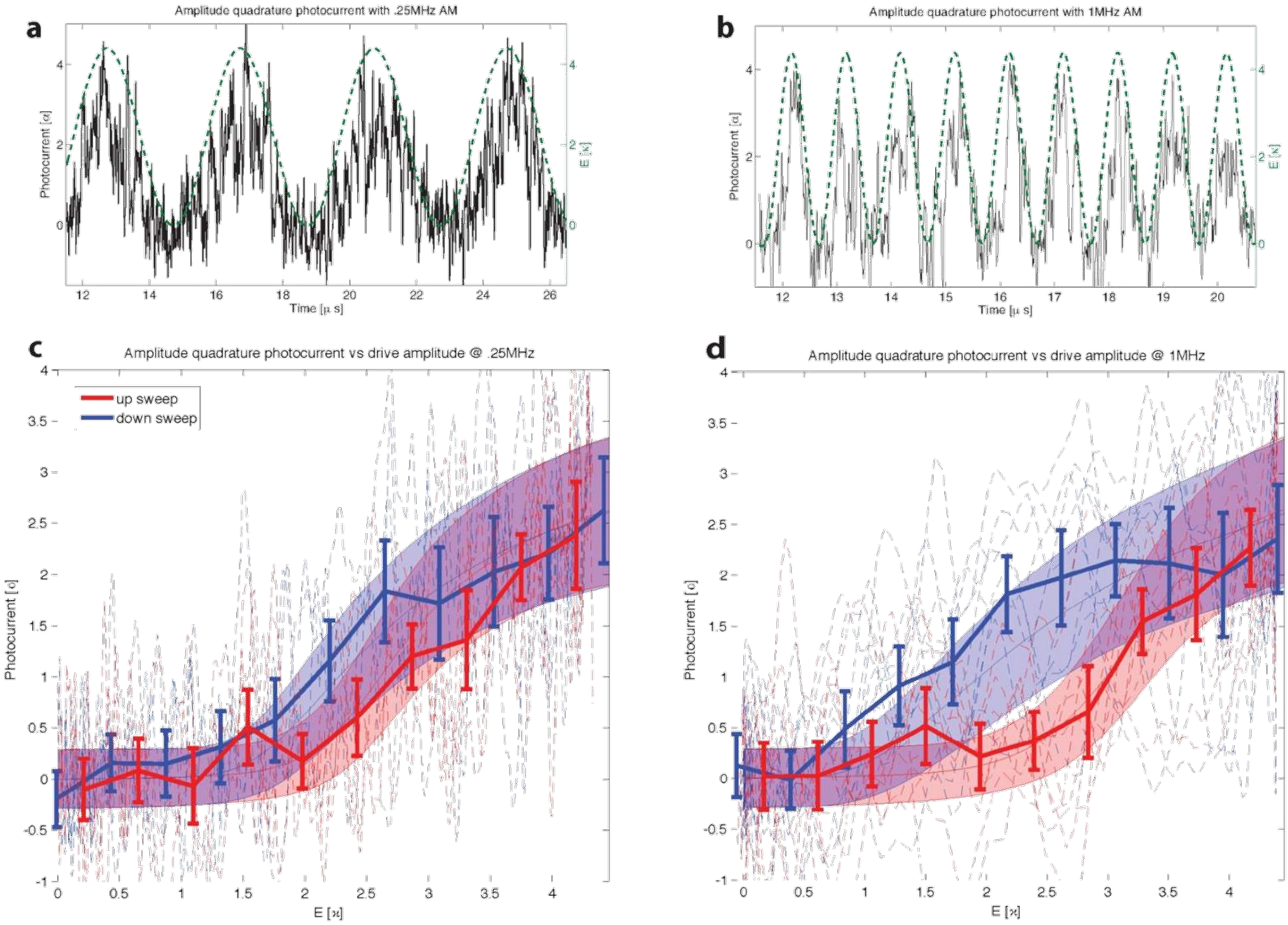






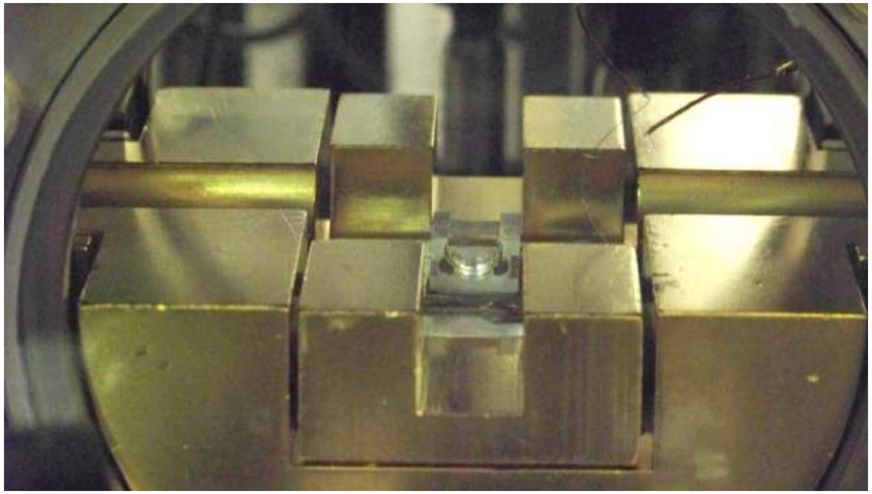
Kinetic (as opposed to equilibrium) hysteresis

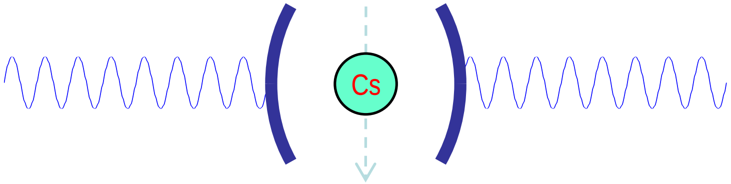
J. Kerckhoff, M. A. Armen and HM, Opt. Express **19**, 24468 (2011)



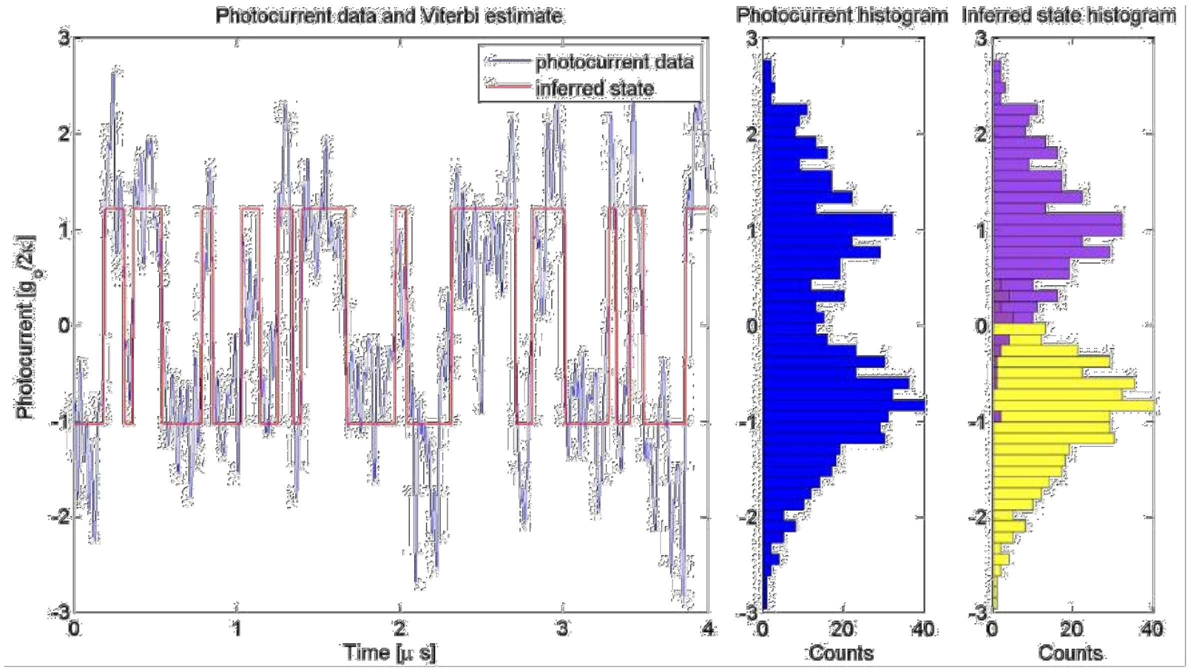
Phase switching in single-atom cavity QED

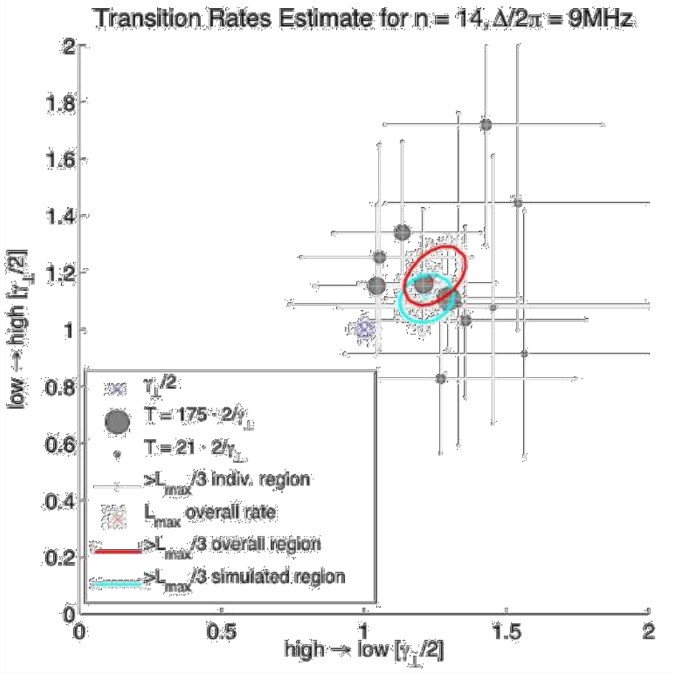
J. Kerckhoff, M. A. Armen, D. S. Pavlichin and HM, Opt. Express **19**, 6478 (2011)



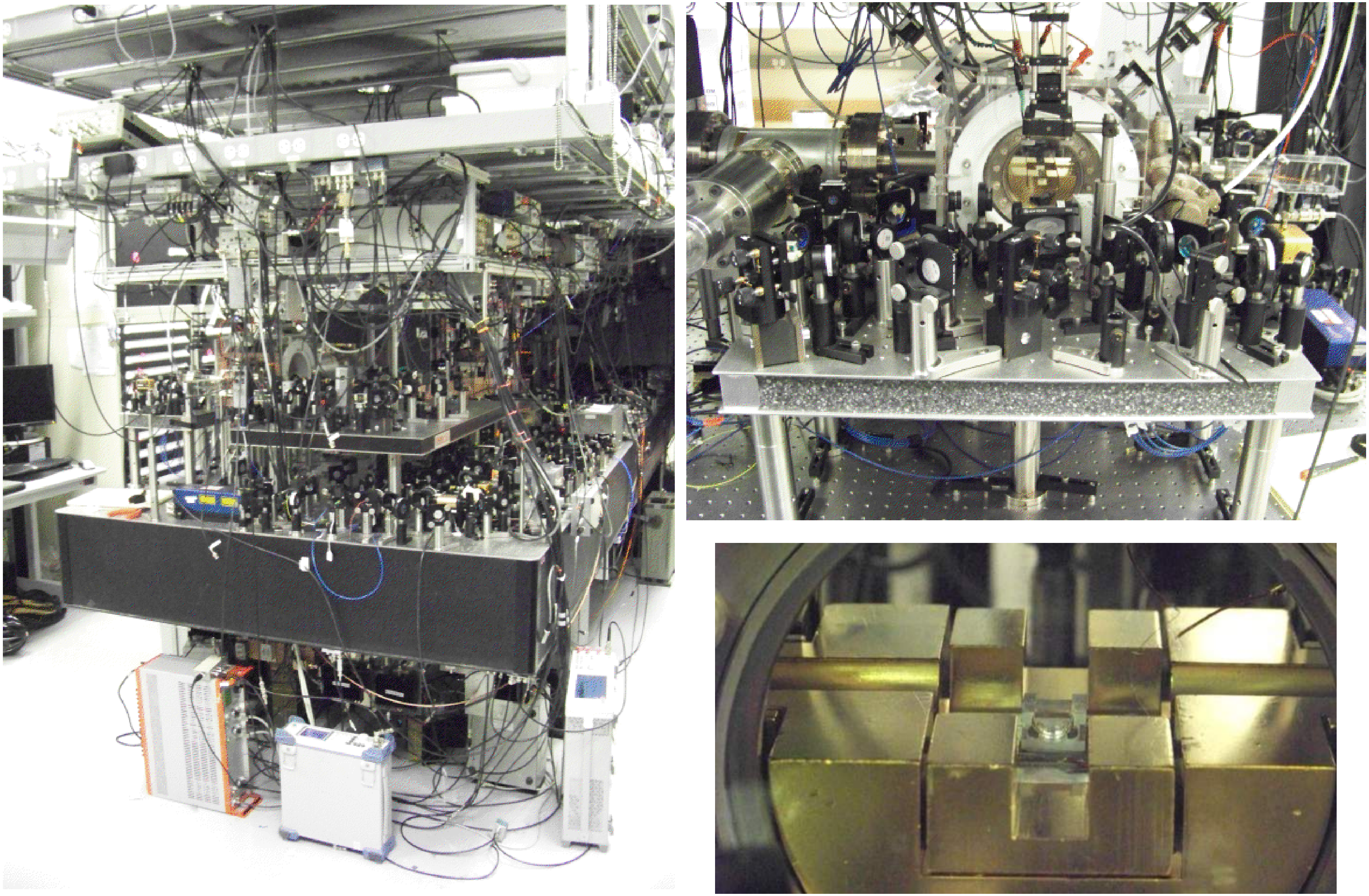


- single-atom cavity QED w/ strong driving
- spontaneous dressed-state polarization
- random binary phase-shift keying
- switching dissipates $\sim$ 0.23 aJ per edge

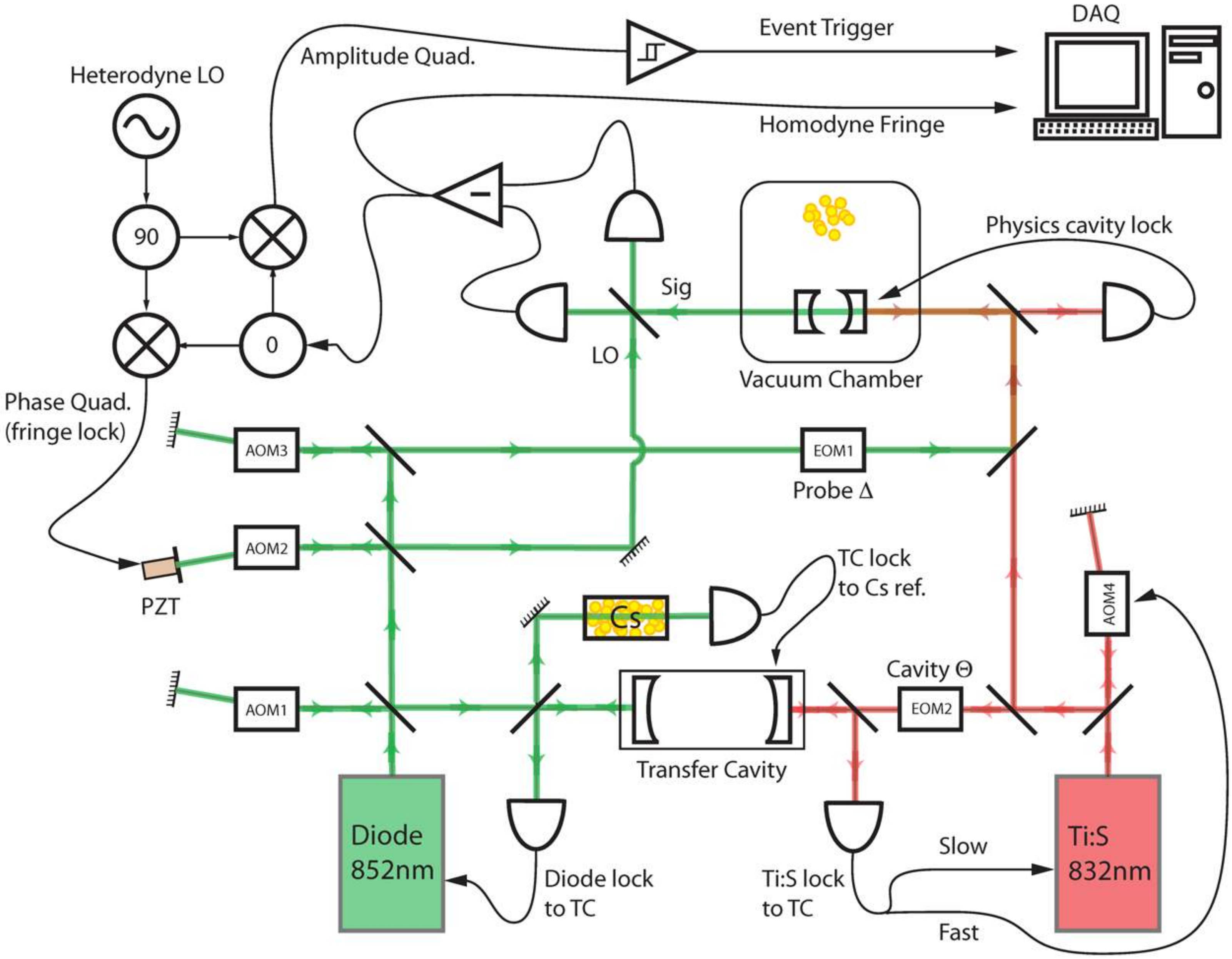




Experimental single-atom cavity QED



Experimental schematic



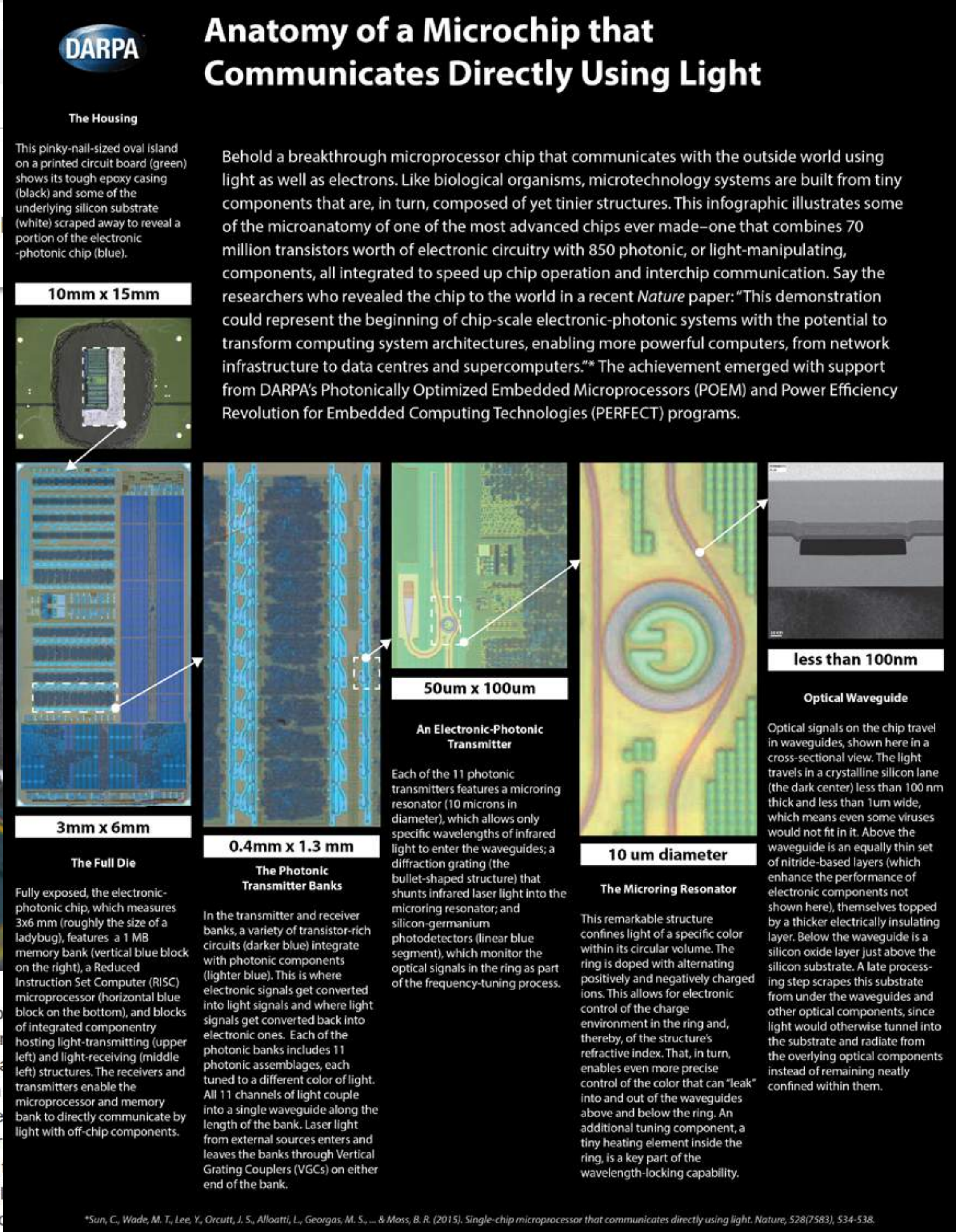
Defense Advanced Research Projects Agency > News And Events

Electricity, Light, Join Forces to Advance Computing

Novel electronic-photonic integrated circuit debuts

OUTREACH@DARPA.MIL
2/19/2016

Integrated circuits traditionally have been a domain reserved for electrons, which co
microscopic structures where the digital calculations and data processing that under
chip designers have been acting on a long-ripening vision of enlisting photons inste
microprocessors. Photons, for one, can serve as fast-as-light carriers of information
brakes on electrons. Recently, DARPA-funded scientists designed and crafted a bre
electrons and photons on a single chip. The result is a remarkable and elegant hybr
of its sub-Lilliputian architecture. To appreciate the engineering acumen involved in
electronic and photonic components, DARPA has produced an annotated, graphical
world of highways, toll gates and traffic circles populated by some of the physical w



Anatomy of a Microchip that Communicates Directly Using Light

Behold a breakthrough microprocessor chip that communicates with the outside world using light as well as electrons. Like biological organisms, microtechnology systems are built from tiny components that are, in turn, composed of yet tinier structures. This infographic illustrates some of the microanatomy of one of the most advanced chips ever made–one that combines 70 million transistors worth of electronic circuitry with 850 photonic, or light-manipulating, components, all integrated to speed up chip operation and interchip communication. Say the researchers who revealed the chip to the world in a recent *Nature* paper: "This demonstration could represent the beginning of chip-scale electronic-photonic systems with the potential to transform computing system architectures, enabling more powerful computers, from network infrastructure to data centres and supercomputers."* The achievement emerged with support from DARPA's Photonically Optimized Embedded Microprocessors (POEM) and Power Efficiency Revolution for Embedded Computing Technologies (PERFECT) programs.

The Housing

This pinky-nail-sized oval island on a printed circuit board (green) shows its tough epoxy casing (black) and some of the underlying silicon substrate (white) scraped away to reveal a portion of the electronic-photonic chip (blue).

10mm x 15mm

3mm x 6mm

The Full Die

Fully exposed, the electronic-photonic chip, which measures 3x6 mm (roughly the size of a ladybug), features a 1 MB memory bank (vertical blue block on the right), a Reduced Instruction Set Computer (RISC) microprocessor (horizontal blue block on the bottom), and blocks of integrated componentry hosting light-transmitting (upper left) and light-receiving (middle left) structures. The receivers and transmitters enable the microprocessor and memory bank to directly communicate by light with off-chip components.

0.4mm x 1.3 mm

The Photonic Transmitter Banks

In the transmitter and receiver banks, a variety of transistor-rich circuits (darker blue) integrate with photonic components (lighter blue). This is where electronic signals get converted into light signals and where light signals get converted back into electronic ones. Each of the photonic banks includes 11 photonic assemblages, each tuned to a different color of light. All 11 channels of light couple into a single waveguide along the length of the bank. Laser light from external sources enters and leaves the banks through Vertical Grating Couplers (VGCs) on either end of the bank.

50um x 100um

An Electronic-Photonic Transmitter

Each of the 11 photonic transmitters features a microring resonator (10 microns in diameter), which allows only specific wavelengths of infrared light to enter the waveguides; a diffraction grating (the bullet-shaped structure) that shunts infrared laser light into the microring resonator; and silicon-germanium photodetectors (linear blue segment), which monitor the optical signals in the ring as part of the frequency-tuning process.

10 um diameter

The Microring Resonator

This remarkable structure confines light of a specific color within its circular volume. The ring is doped with alternating positively and negatively charged ions. This allows for electronic control of the charge environment in the ring and, thereby, of the structure's refractive index. That, in turn, enables even more precise control of the color that can "leak" into and out of the waveguides above and below the ring. An additional tuning component, a tiny heating element inside the ring, is a key part of the wavelength-locking capability.

less than 100nm

Optical Waveguide

Optical signals on the chip travel in waveguides, shown here in a cross-sectional view. The light travels in a crystalline silicon lane (the dark center) less than 100 nm thick and less than 1um wide, which means even some viruses would not fit in it. Above the waveguide is an equally thin set of nitride-based layers (which enhance the performance of electronic components not shown here), themselves topped by a thicker electrically insulating layer. Below the waveguide is a silicon oxide layer just above the silicon substrate. A late processing step scrapes this substrate from under the waveguides and other optical components, since light would otherwise tunnel into the substrate and radiate from the overlying optical components instead of remaining neatly confined within them.

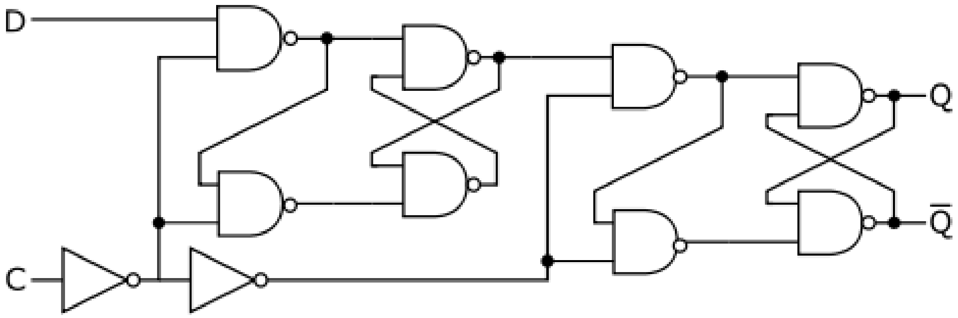
**Sun, C., Wade, M. T., Lee, Y., Orcutt, J. S., Alloatti, L., Georgas, M. S., ... & Moss, B. R. (2015). Single-chip microprocessor that communicates directly using light. Nature, 528(7583), 534-538.*

Ultra-low power nanophotonic circuit theory

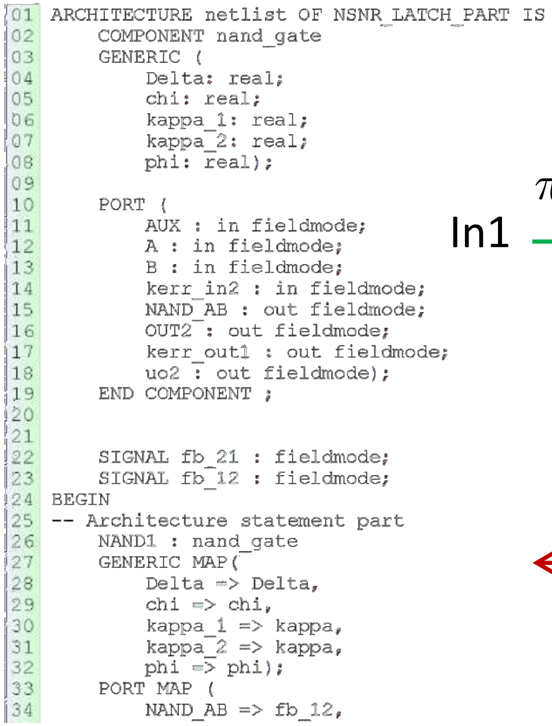
HM, Appl. Phys. Lett. **98**, 193109 & **99**, 153103 (2011)

PLINC: Photonic Logic via Interferometry with Nonlinear Components

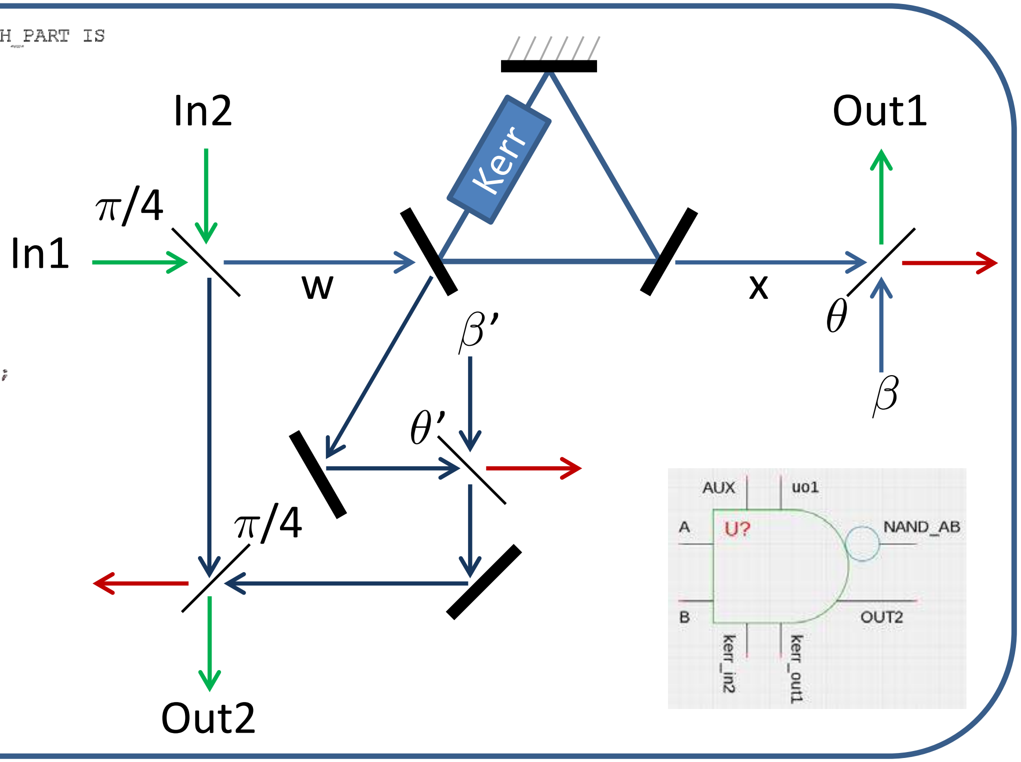
- PLINC exploits *cavity-enhanced nonlinearity* and *circuit-scale optical coherence* to implement attojoule photonic logic
- PLINC is a natural scheme for near-future integrated nanophotonics, testable today using single-atom cavity QED
- **PLINC circuit theory = coherent-feedback quantum control**



1. Develop QHDL, a subset of industry-standard VHDL for the specification of PLINC circuits
2. Develop software for compiling QHDL into rigorous quantum optical models
3. Use QHDL toolbox + high-performance numerical simulation for analysis and design of functional circuits
4. Validate key coherent feedback concepts in single-atom cavity QED experiments

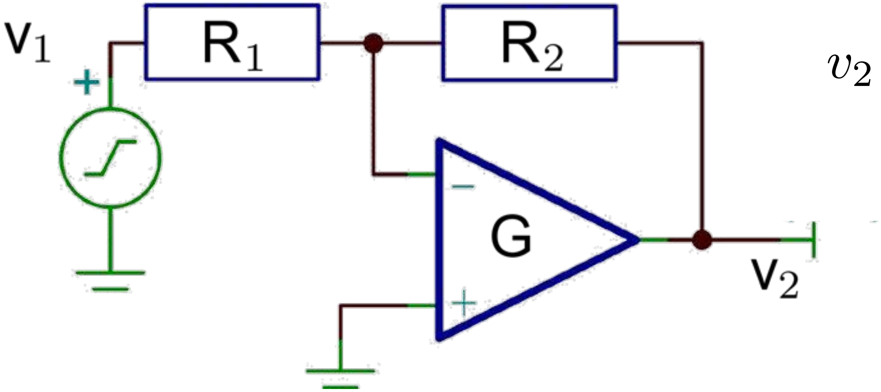


```
ARCHITECTURE netlist OF NSNR_LATCH_PART IS
    COMPONENT nand_gate
    GENERIC (
        Delta: real;
        chi: real;
        kappa_1: real;
        kappa_2: real;
        phi: real);

    PORT (
        AUX : in fieldmode;
        A : in fieldmode;
        B : in fieldmode;
        kerr_in2 : in fieldmode;
        NAND_AB : out fieldmode;
        OUT2 : out fieldmode;
        kerr_out1 : out fieldmode;
        uo2 : out fieldmode);
    END COMPONENT ;


    SIGNAL fb_21 : fieldmode;
    SIGNAL fb_12 : fieldmode;
BEGIN
-- Architecture statement part
    NAND1 : nand_gate
    GENERIC MAP(
        Delta => Delta,
        chi => chi,
        kappa_1 => kappa,
        kappa_2 => kappa,
        phi => phi);
    PORT MAP (
        NAND_AB => fb_12,
```



Feedback (control) motifs in circuit design

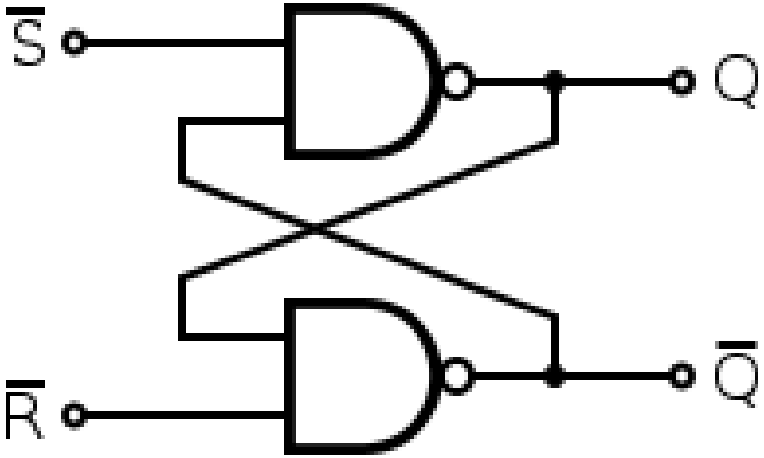
Stabilization (robustness)



http://www.rfdesignline.com/howto/209400216

$$
\begin{aligned}
v_2 &= -v_1 \frac{GR_2}{R_1 + R_2 + GR_1} \\
&\to -\frac{R_2}{R_1} v_1
\end{aligned}
$$

Synthesis

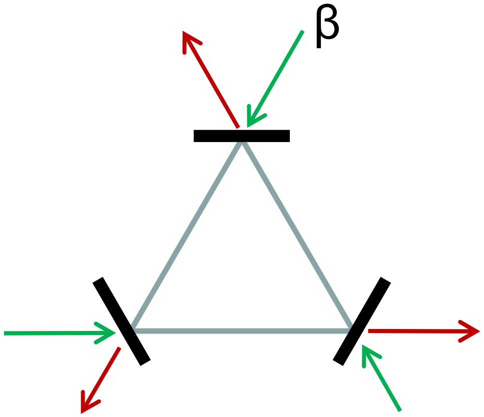


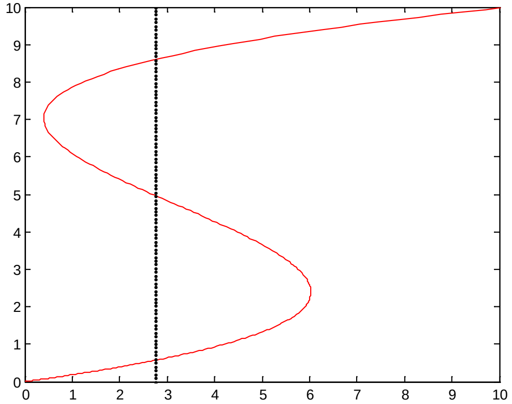
$\overline{S}$	$\overline{R}$	Q
1	1	*hold*
0	1	→ 1
1	0	→ 0
0	0	*undef*

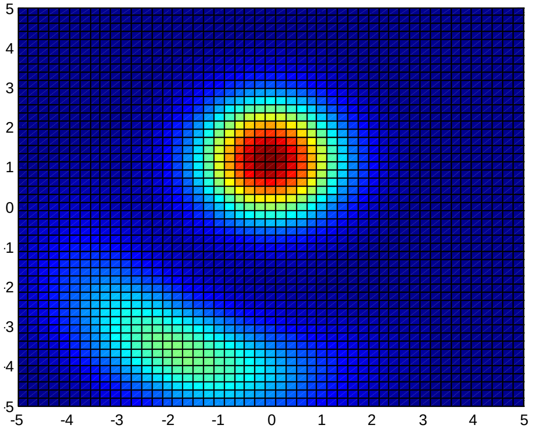
Steady-state analysis can be intuitive, but need theory for dynamics (transients), noise

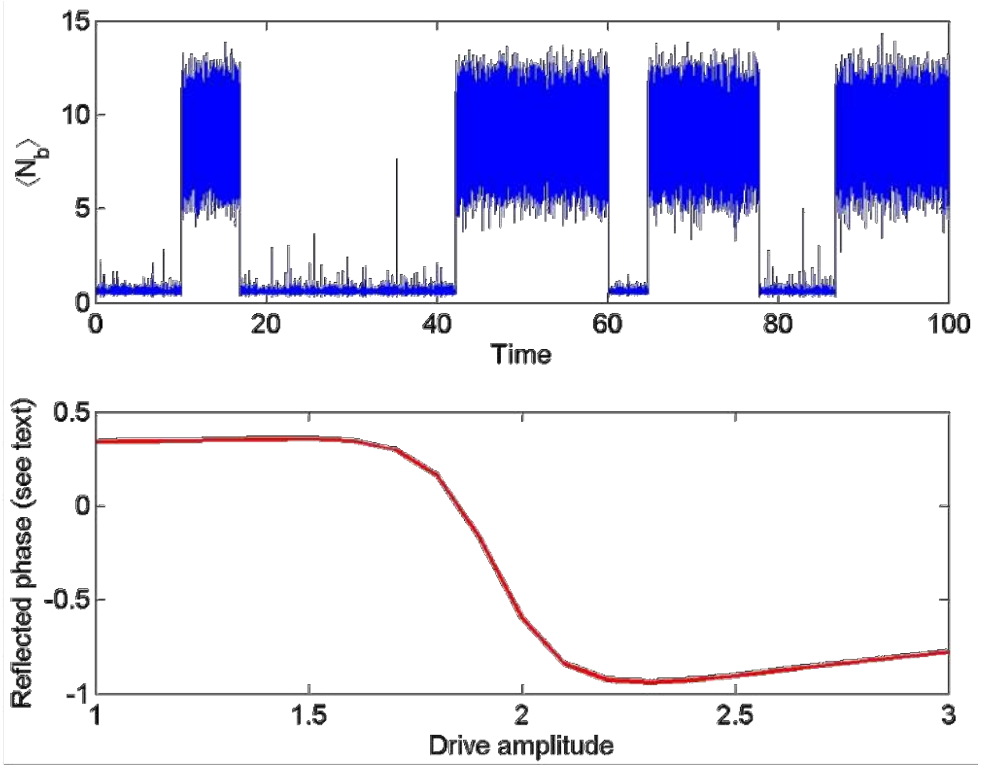
Attojoule nanophotonic switch stabilization

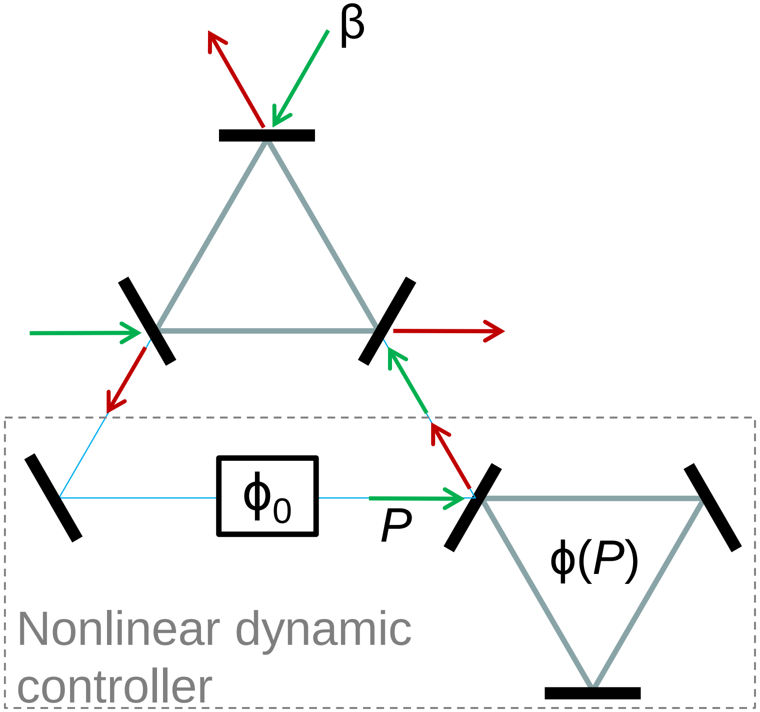
HM, Appl. Phys. Lett. **98**, 193109 (2011)







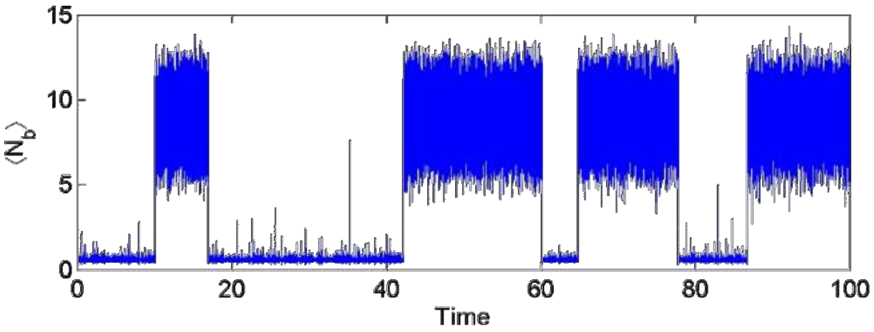


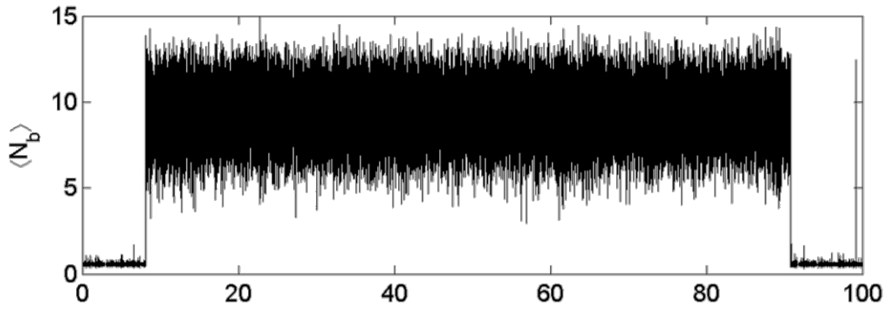


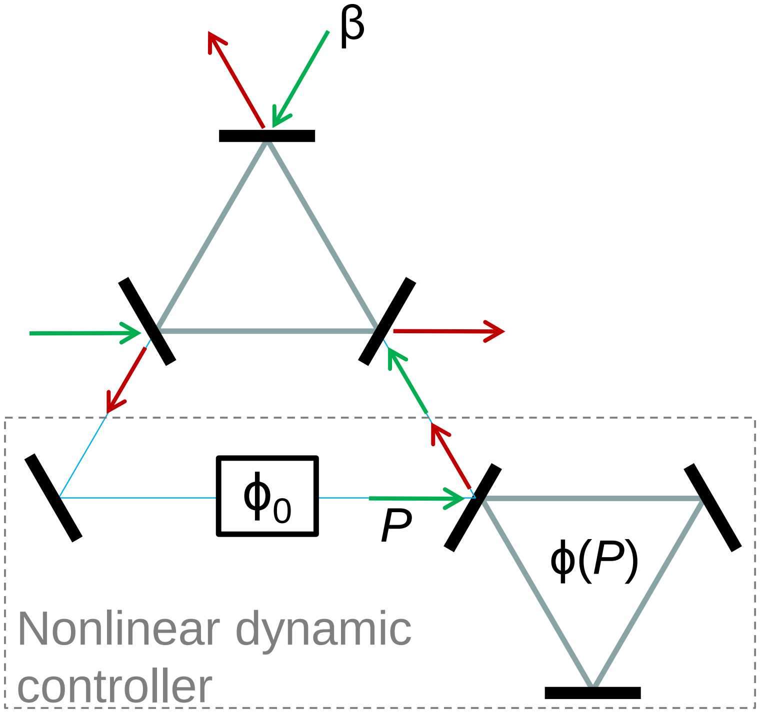
Nonlinear dynamic controller

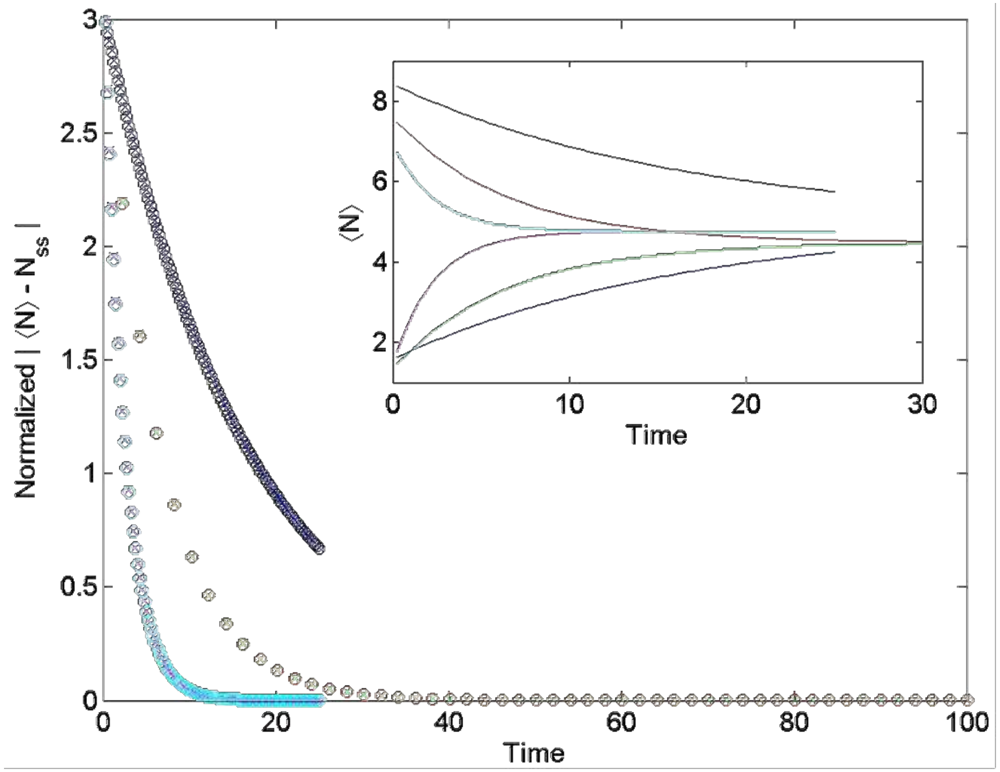
Attojoule nanophotonic switch stabilization

HM, Appl. Phys. Lett. **98**, 193109 (2011)







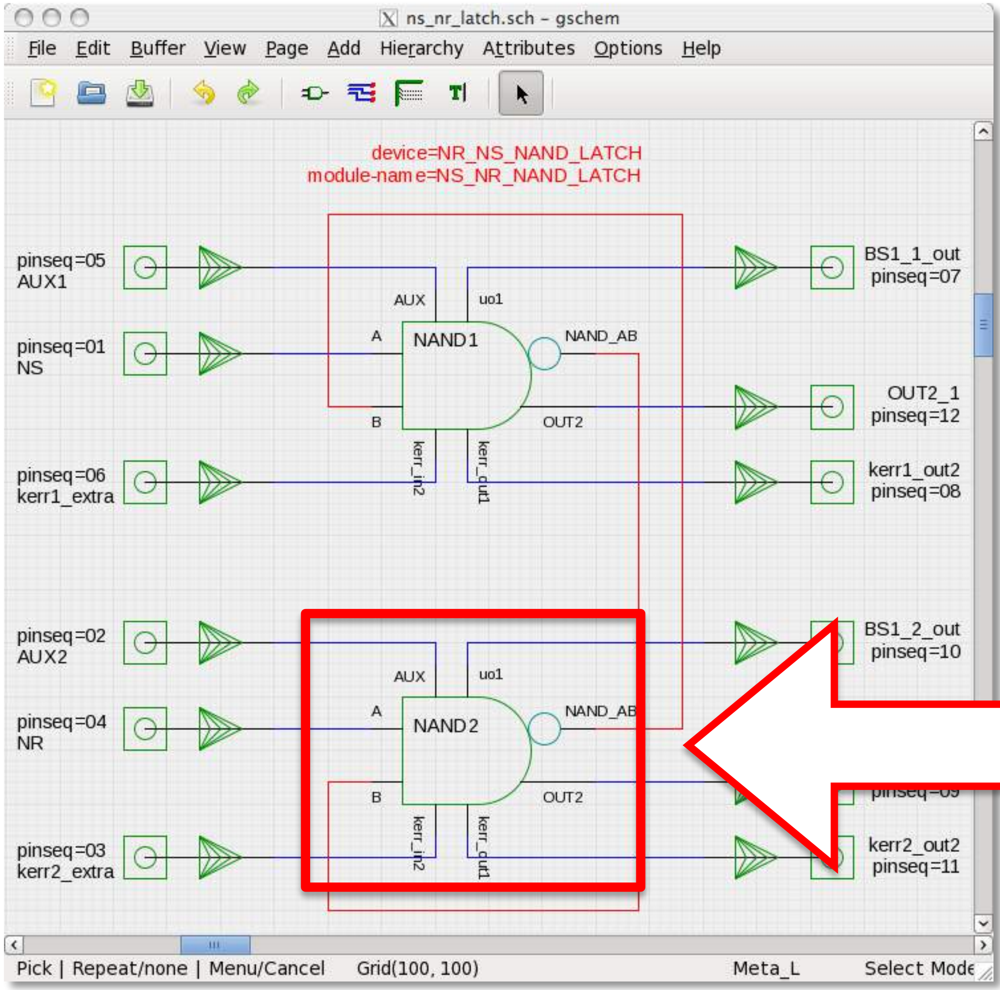


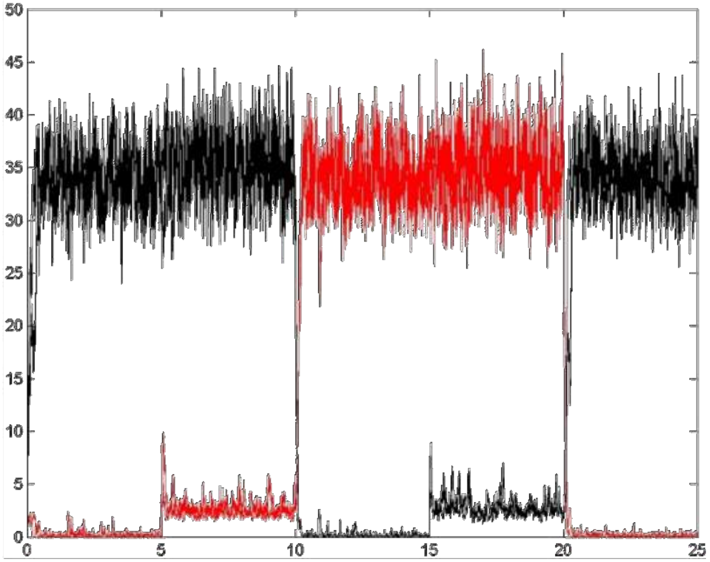
Quantum models for attojoule photonic switching

HM, Appl. Phys. Lett. **99**, 153103 (2011)

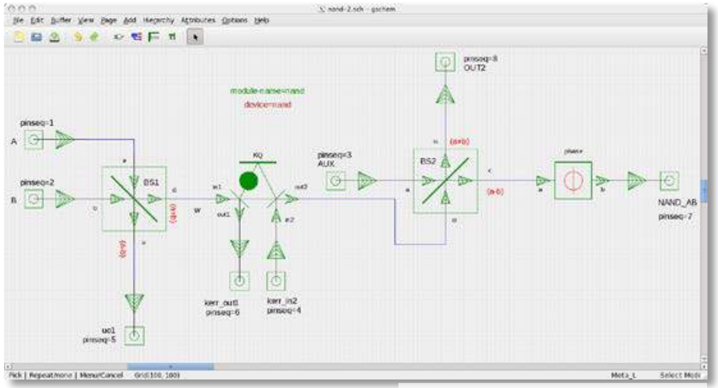
N. Tezak, A. Niederberger, D. S. Pavlichin, G. Sarma and HM, Phil. Trans. Roy. Soc. A **370**, 5270 (2012)

SR NAND latch





Hierarchical Design



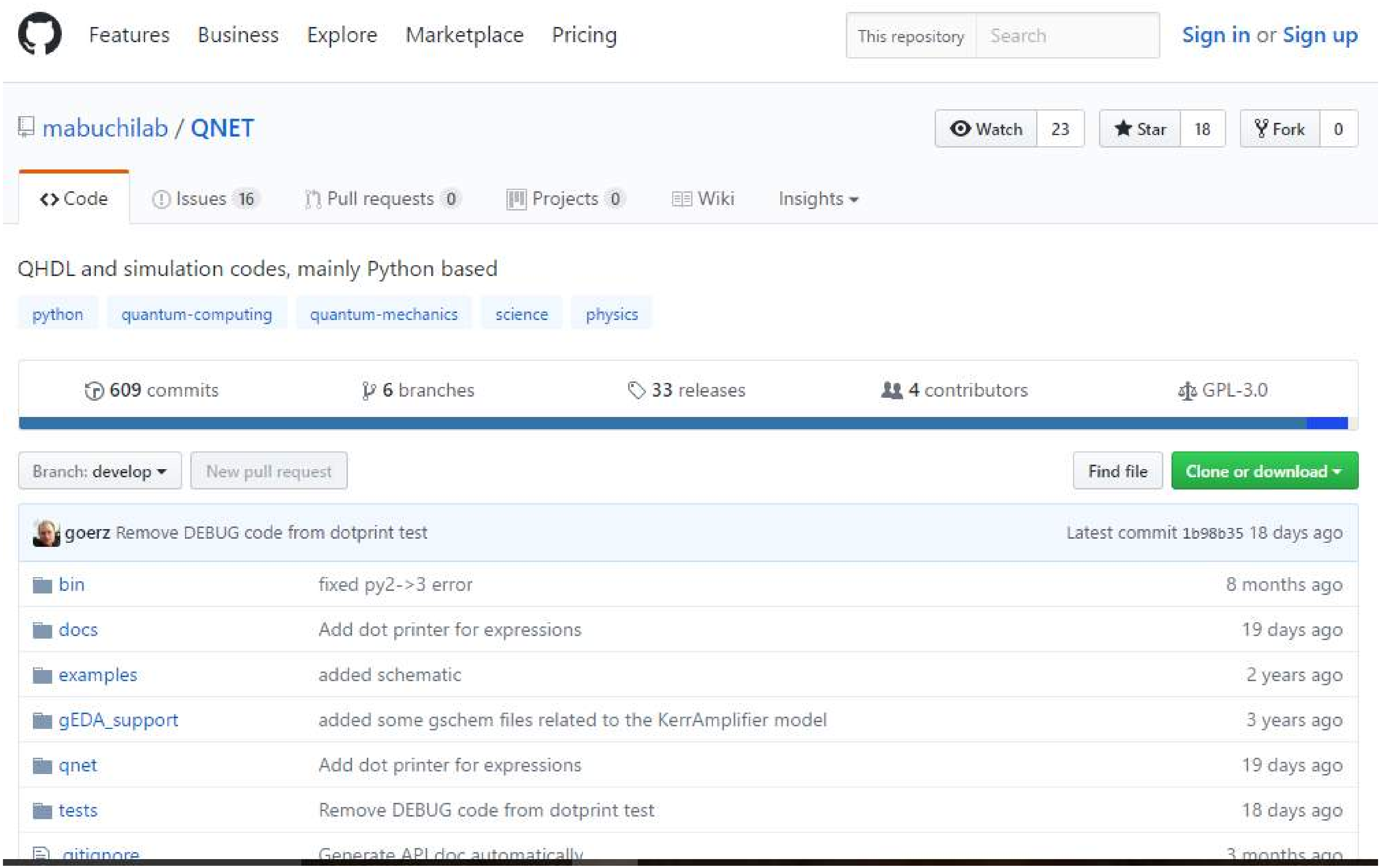
NAND gate

http://mabuchilab.github.com/QNET/

The QNET simulation package (GitHub)

N. Tezak, A. Niederberger, D. S. Pavlichin, G. Sarma and HM, Phil. Trans. Roy. Soc. A **370**, 5270 (2012)

*** Interaction with ARL/CDQI ***



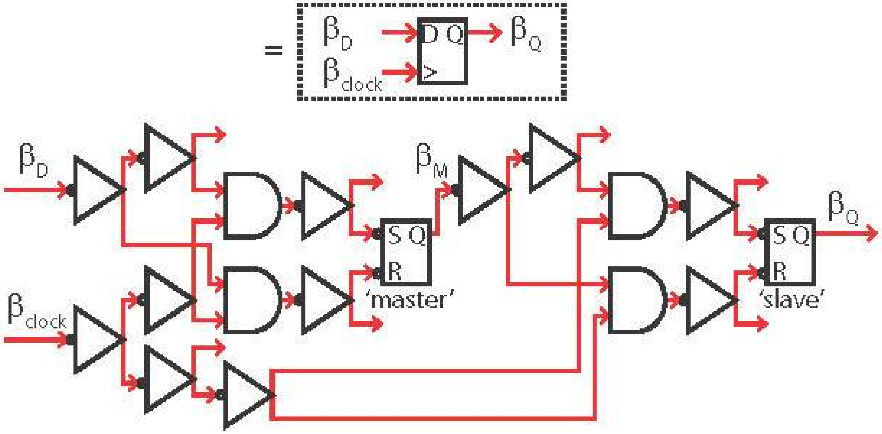
QHDL and simulation codes, mainly Python based

goerz Remove DEBUG code from dotprint test — Latest commit 1b98b35 18 days ago

bin	fixed py2->3 error	8 months ago
docs	Add dot printer for expressions	19 days ago
examples	added schematic	2 years ago
gEDA_support	added some gschem files related to the KerrAmplifier model	3 years ago
qnet	Add dot printer for expressions	19 days ago
tests	Remove DEBUG code from dotprint test	18 days ago
.gitignore	Generate API doc automatically	3 months ago

Quantum noise in large-scale coherent circuits

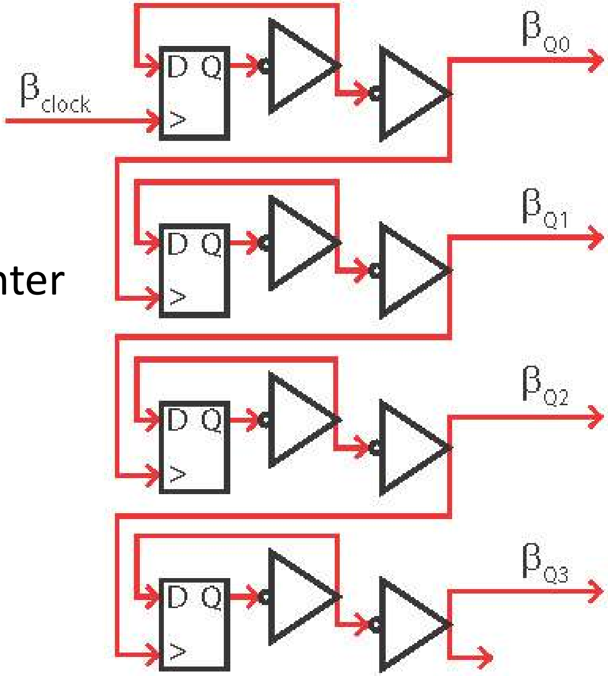
C. Santori *et al.* (HP Labs + Stanford), Phys. Rev. Appl. **1**, 054005 (2014)

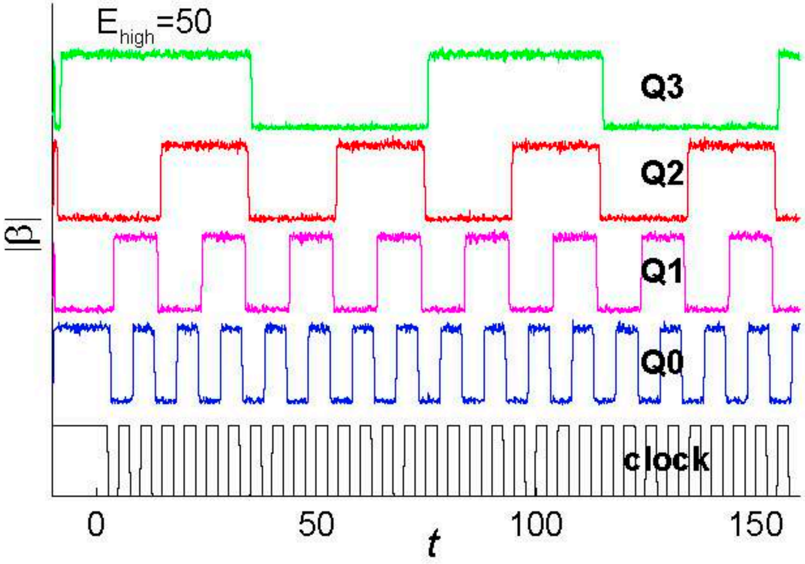


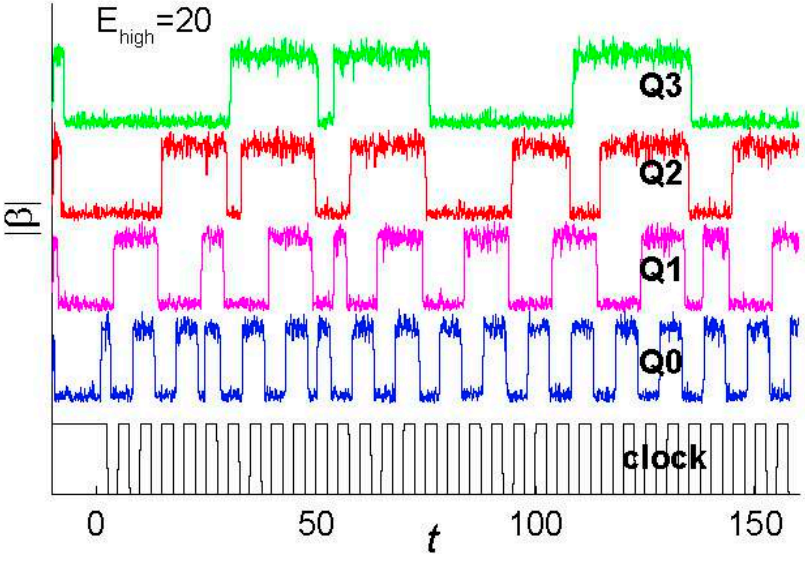
4-bit ripple counter

= 4 flip-flops

= 88 resonators

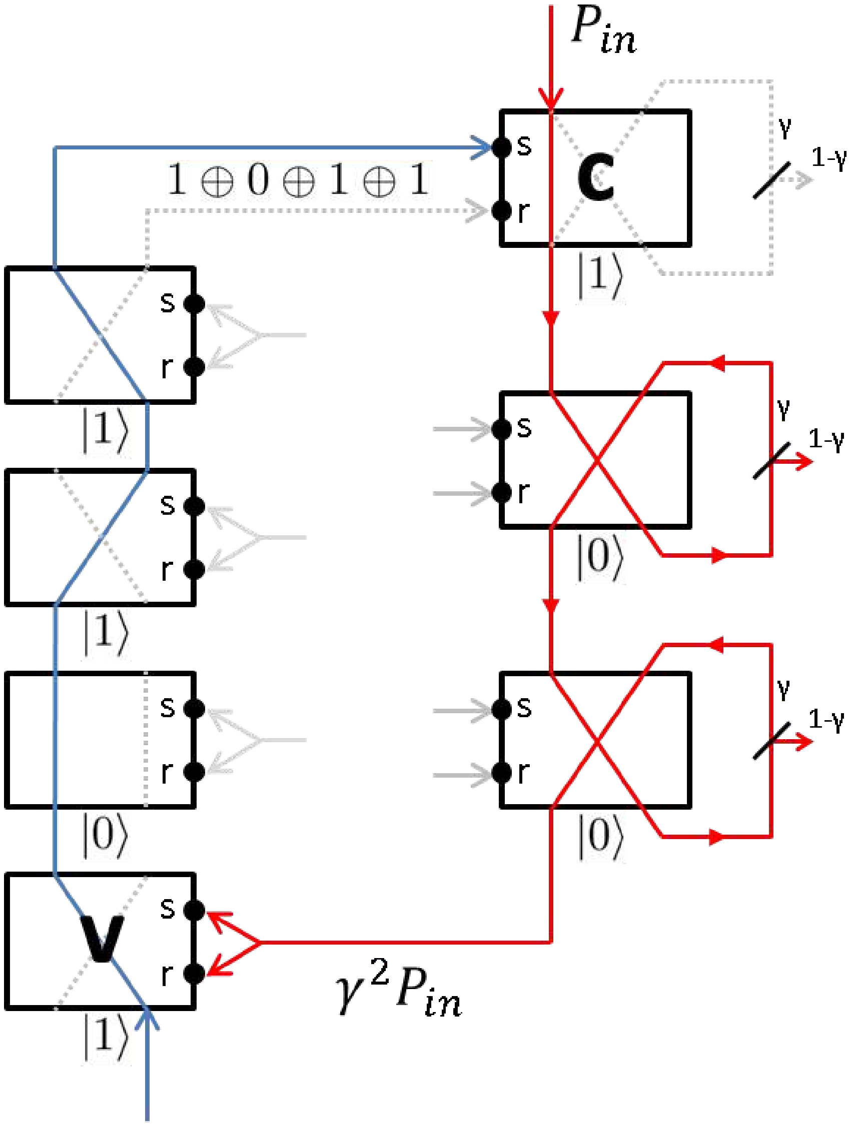


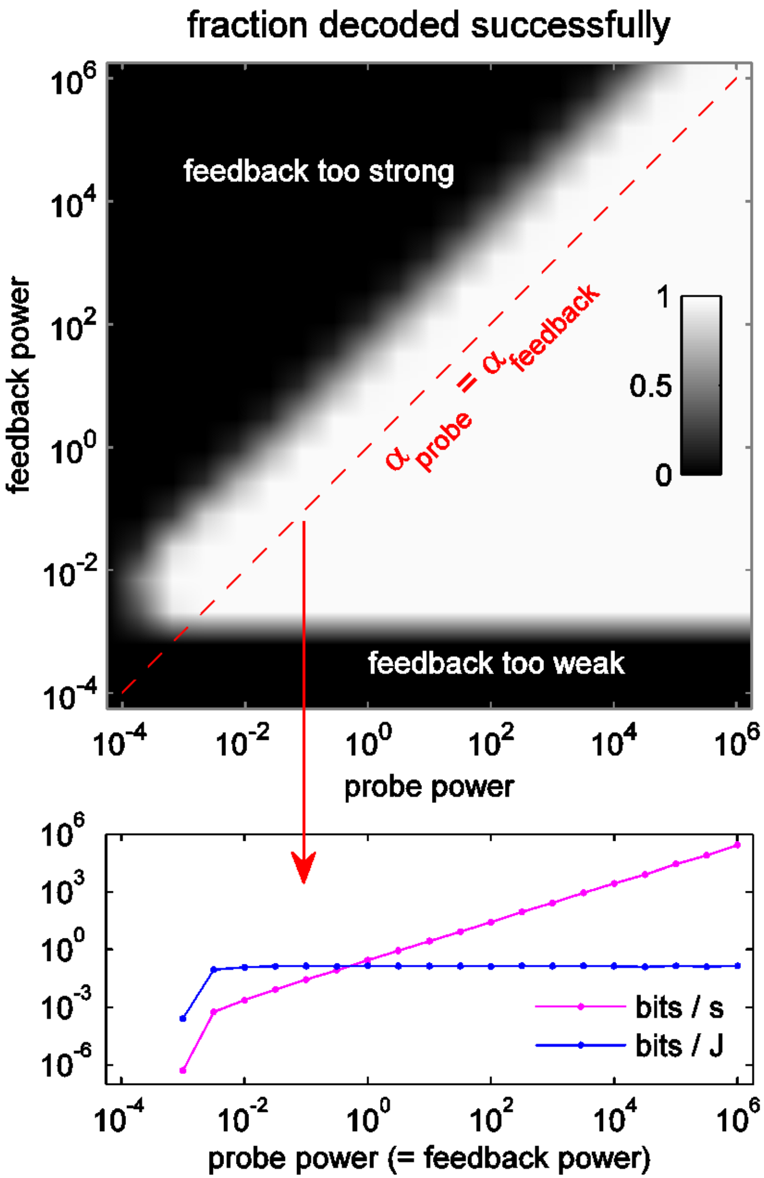




Message passing in nanophotonic circuits

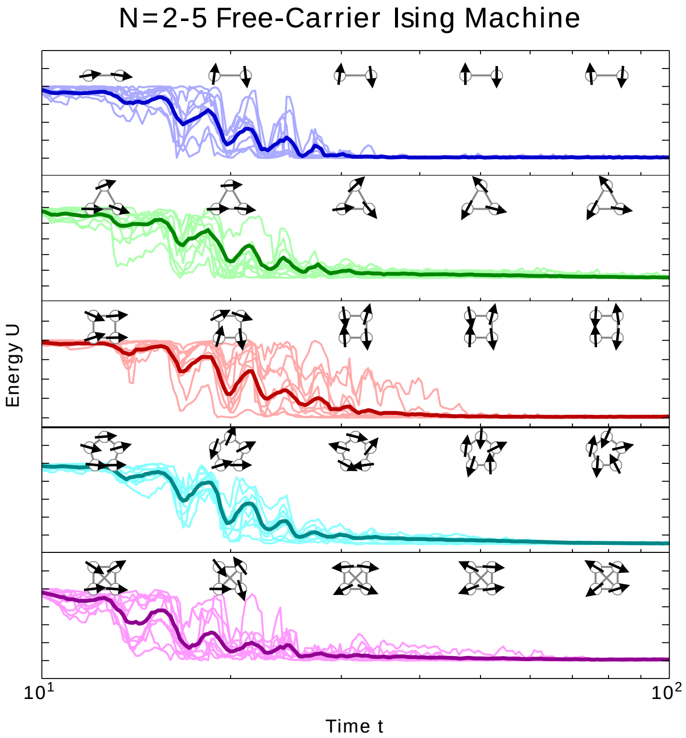
D. Pavlichin and HM, New J. Phys. **16**, 105017 (2014)

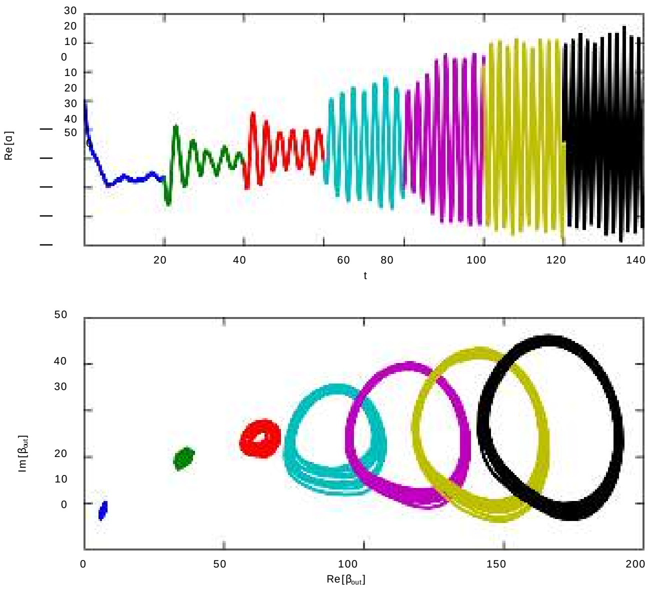


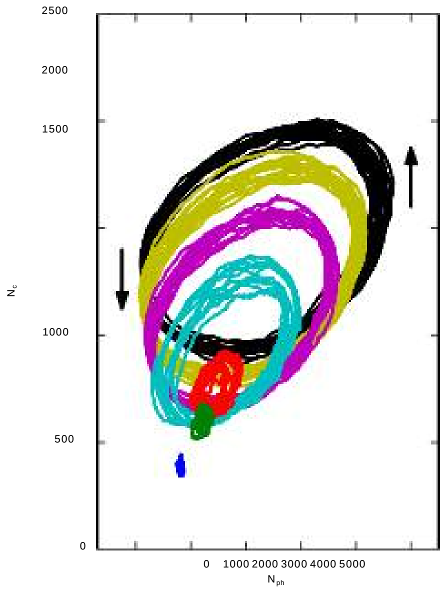


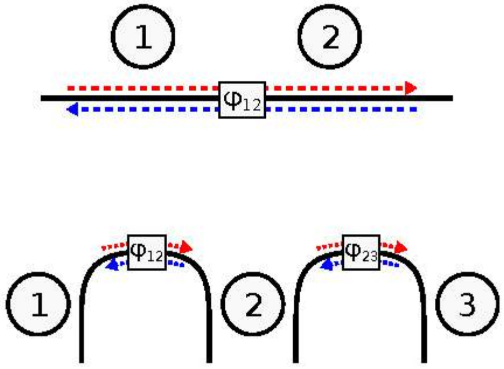
Limit-cycle oscillators, synchronization and Ising-XY

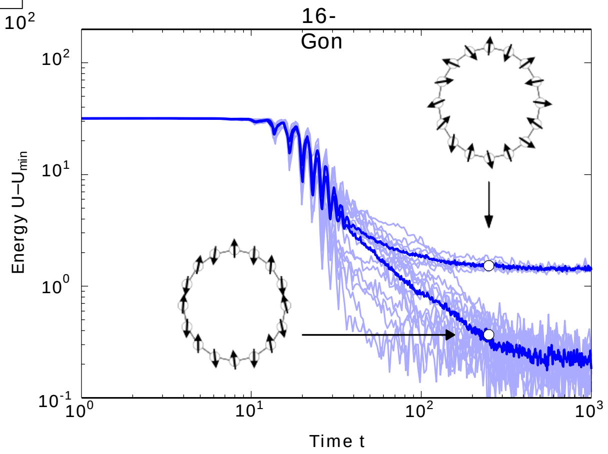
Ryan Hamerly and HM, Phys. Rev. Appl. 4, 024016 (2015)

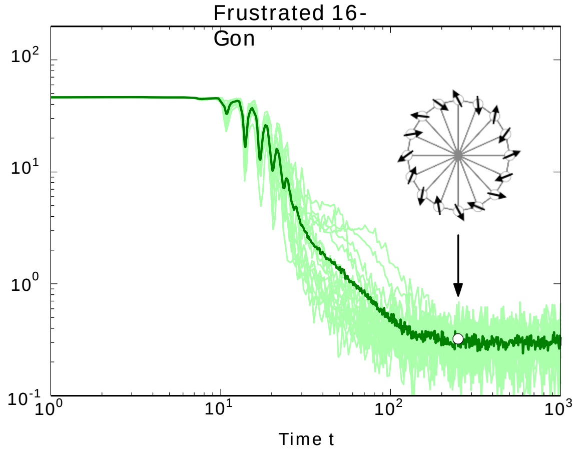

N=2-5 Free-Carrier Ising Machine







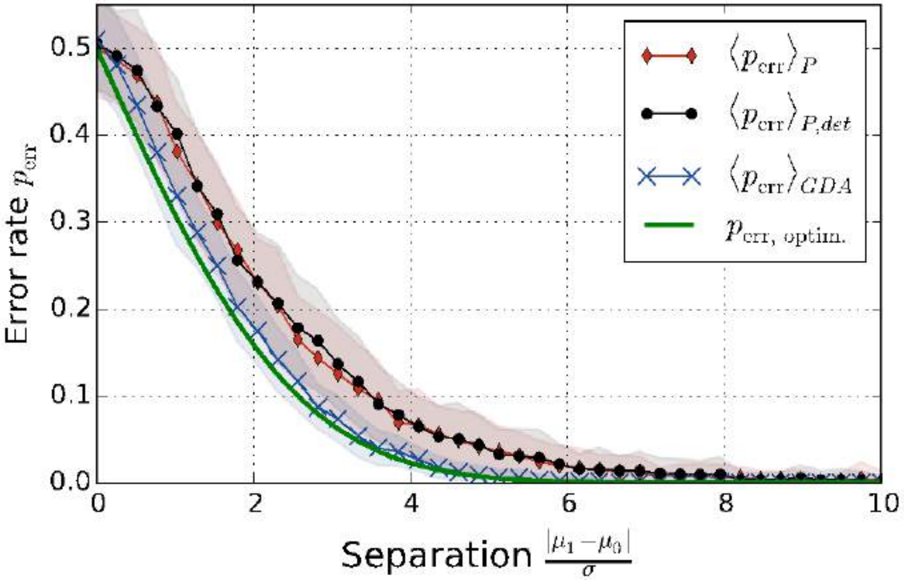

16-Gon

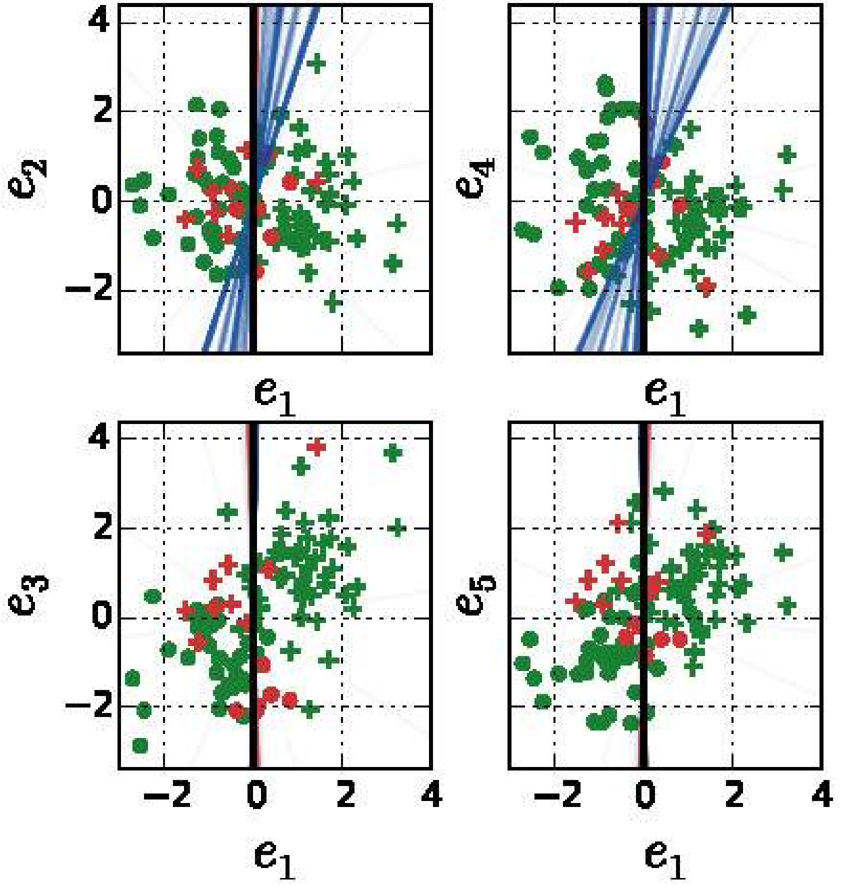

Frustrated 16-Gon

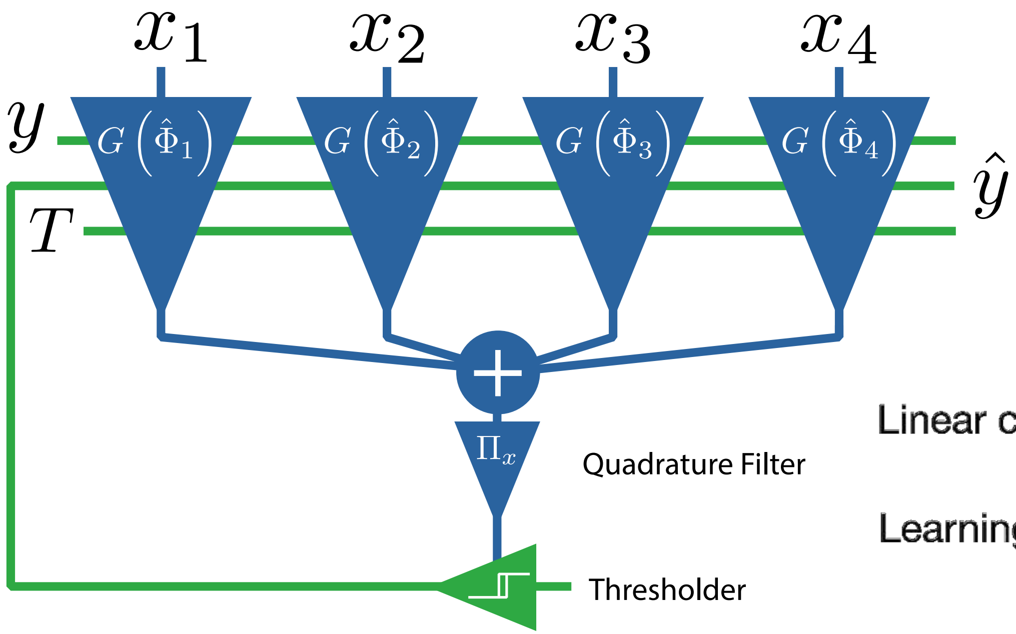
Role of entanglement? Y. Yamamoto et al., PRA **92**, 043821

Coherent perceptron for all-optical machine learning

N. Tezak and HM, EPJ Quantum Technology **2**:10 (2015)







Linear classifier

$$\hat{y}_w[x] := \theta(w^T x) = \begin{cases} 1 \text{ for } w^T x \geq 0 \\ 0 \text{ otherwise.} \end{cases}$$

Learning rule

$$\Delta w = \tilde{\alpha}\left(y^{(j)} - \hat{y}_w[x^{(j)}]\right) x^{(j)}$$